# Octal 3-State Non-Inverting D Flip-Flop

## High−Performance Silicon−Gate CMOS

# MC74HC374A, MC74HCT374A

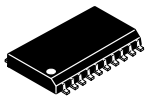
The MC74HC374A/MC74HCT374A is identical in pinout to the LS374. The MC74HC374A inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs. The MC74HCT374A may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

Data meeting the set−up time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip−flops but when Output Enable is high, all device outputs are forced to the high−impedance state. Thus, data may be stored even when the outputs are not enabled.

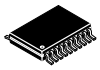
The HC374A/HCT374A is identical in function to the HC574A/HCT574A which has the input pins on the opposite side of the package from the output. This device is similar in function to the HC534A/HCT534A which has inverting outputs.

### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 276 FETs or 69 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

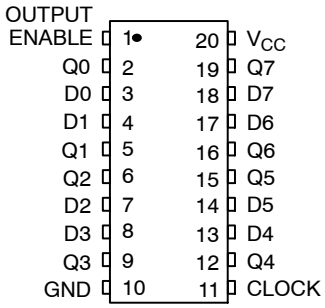


**SOIC−20**
**DW SUFFIX**
**CASE 751D**

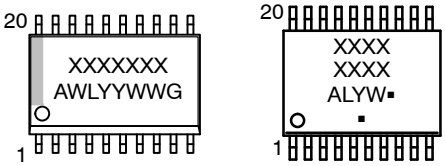


**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

### PIN ASSIGNMENT




### MARKING DIAGRAMS




**SOIC−20** **TSSOP−20**

| | |
|---|---|
| XXXXXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| **Output Enable** | **Clock** | **D** | **Q** |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L,H,↓ | X | No Change |
| H | X | X | Z |

X = don't care
Z = high impedance

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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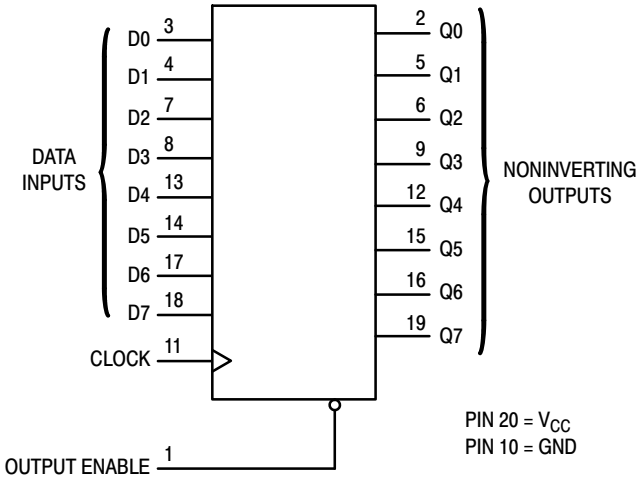



**Figure 1. Logic Diagram**

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to $V_{CC}$+0.5 | V |
| $V_{OUT}$ | DC Output Voltage | | −0.5 to $V_{CC}$+0.5 | V |
| $I_{IN}$ | DC Input Diode Current, per Pin | | ±20 | mA |
| $I_{OUT}$ | DC Input Diode Current, Per Pin | | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ±75 | mA |
| $I_{IK}$ | Input Clamp Current ($V_{IN}$ < 0 or $V_{IN}$ > $V_{CC}$) | | ±20 | mA |
| $I_{OK}$ | Output Clamp Current ($V_{OUT}$ < 0 or $V_{OUT}$ > $V_{CC}$) | | ±20 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 1) | SOIC−20W<br>WQFN20<br>QFN20<br>TSSOP−20 | 96<br>99<br>111<br>150 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 25°C | SOIC−20W<br>WQFN20<br>QFN20<br>TSSOP−20 | 1302<br>1256<br>1127<br>833 | mW |
| MSL | Moisture Sensitivity | | Level 1 | − |
| $F_R$ | Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | − |
| $V_{ESD}$ | ESD Withstand Voltage (Note 2) | Human Body Model<br>Charged Device Model | > 2000<br>> 1000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| **MC74HC** | | | | | |
| $V_{CC}$ | DC Supply Voltage | | 2.0 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Note 3) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time | $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |
| **MC74HCT** | | | | | |
| $V_{CC}$ | DC Supply Voltage | | 4.5 | 5.5 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Note 3) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Free−Air Temperature | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time | | 0 | 500 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (MC74HC374A)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | −55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20$ μA | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20$ μA | 2.0<br>3.0<br>4.5<br>6.0 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20$ μA | 2.0<br>4.5<br>6.0 | 1.90<br>4.40<br>5.90 | 1.90<br>4.40<br>5.90 | 1.90<br>4.40<br>5.90 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 2.4$ mA<br>$\|I_{out}\| \le 6.0$ mA<br>$\|I_{out}\| \le 7.8$ mA | 3.0<br>4.5<br>6.0 | 2.48<br>2.98<br>5.48 | 2.34<br>3.84<br>5.34 | 2.20<br>3.70<br>5.20 | V |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20$ μA | 2.0<br>4.5<br>6.0 | 0.10<br>0.10<br>0.10 | 0.10<br>0.10<br>0.10 | 0.10<br>0.10<br>0.10 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 2.4$ mA<br>$\|I_{out}\| \le 6.0$ mA<br>$\|I_{out}\| \le 7.8$ mA | 3.0<br>4.5<br>6.0 | 0.26<br>0.26<br>0.26 | 0.33<br>0.33<br>0.33 | 0.40<br>0.40<br>0.40 | V |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three−State Leakage Current | Output in High−Impedance State<br>$V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 6.0 | 4 | 40 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**AC ELECTRICAL CHARACTERISTICS** (MC74HC374A)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) | 2.0<br>3.0<br>4.5<br>6.0 | 6<br>15<br>30<br>35 | 5<br>10<br>24<br>28 | 4<br>8<br>20<br>24 | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Maximum Propagation Delay, Input Clock to Q (Figures 2 and 3) | 2.0<br>3.0<br>4.5<br>6.0 | 125<br>80<br>25<br>21 | 155<br>110<br>31<br>26 | 190<br>130<br>38<br>32 | ns |
| $t_{PLZ}$<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Q (Figures 2 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 150<br>100<br>30<br>26 | 190<br>125<br>38<br>33 | 225<br>150<br>45<br>38 | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to Q (Figures 2 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 150<br>100<br>30<br>26 | 190<br>125<br>38<br>33 | 225<br>150<br>45<br>38 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 3) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13 | 95<br>32<br>19<br>16 | 110<br>36<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three–State Output Capacitance (Output in High–Impedance State) | | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output)* | 34 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**TIMING REQUIREMENTS** (MC74HC374A)

| Symbol | Parameter | Figure | $V_{CC}$ V | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{su}$ | Minimum Setup Time, Data to Clock | 5 | 2.0<br>3.0<br>4.5<br>6.0 | 50<br>40<br>10<br>9 | | 65<br>50<br>13<br>11 | | 75<br>60<br>15<br>13 | | ns |
| $t_h$ | Minimum Hold Time, Clock to Data | 5 | 2.0<br>3.0<br>4.5<br>6.0 | 5.0<br>5.0<br>5.0<br>5.0 | | 5.0<br>5 0<br>5.0<br>5.0 | | 5.0<br>5.0<br>5.0<br>5.0 | | ns |
| $t_w$ | Minimum Pulse Width, Clock | 2 | 2.0<br>3.0<br>4.5<br>6.0 | 60<br>23<br>12<br>10 | | 75<br>27<br>15<br>13 | | 90<br>32<br>18<br>15 | | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | 2 | 2.0<br>3.0<br>4.5<br>6.0 | | 1000<br>800<br>500<br>400 | | 1000<br>800<br>500<br>400 | | 1000<br>800<br>500<br>400 | ns |

**DC ELECTRICAL CHARACTERISTICS** (MC74HCT374A)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 6.0$ mA | 4.5 | 3.98 | 3.84 | 3.7 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 6.0$ mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 5.5 | 4.0 | 40 | 160 | μA |
| $I_{OZ}$ | Maximum Three–State Leakage Current | $V_{in}$ = $V_{IL}$ or $V_{IH}$ (Note 4)<br>$V_{out}$ = $V_{CC}$ or GND | 5.5 | –0.5 | –5.0 | –10 | μA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4 V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0 μA | | ≥ –55°C | 25°C to 125°C | | |
| | | | 5.5 | 2.9 | 2.4 | | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Output in high–impedance state.

**AC ELECTRICAL CHARACTERISTICS** (MC74HCT374A)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $f_{MAX}$ | Maximum Clock Frequency (50% Duty Cycle) | 30 | 24 | 20 | MHz |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Clock to Q | 30 | 38 | 45 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Q | 28 | 35 | 42 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Propagation Delay Time, Output Enable to Q | 28 | 35 | 42 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output | 12 | 15 | 18 | ns |
| $C_{in}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |

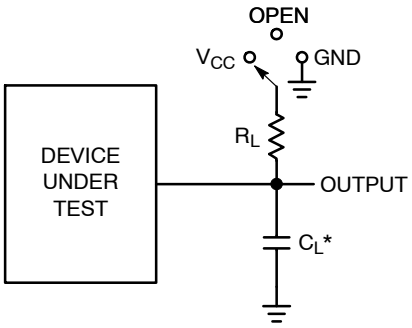
| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Flip–Flop)* | 58 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**TIMING REQUIREMENTS** (MC74HCT374A)

| Symbol | Parameter | Guaranteed Limit | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | – 55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{su}$ | Minimum Setup Time, Data to Clock | 10 | | 13 | | 15 | | ns |
| $t_h$ | Minimum Hold Time, Clock to Data | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_w$ | Minimum Pulse Width, Clock | 15 | | 19 | | 22 | | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | | 500 | | 500 | | 500 | ns |

## SWITCHING WAVEFORMS




*$C_L$ Includes probe and jig capacitance

| Test | Switch Position | $C_L$ | $R_L$ |
|---|---|---|---|
| $t_{PLH}$ / $t_{PHL}$ | Open | 50 pF | 1 kΩ |
| $t_{PLZ}$ / $t_{PZL}$ | $V_{CC}$ | | |
| $t_{PHZ}$ / $t_{PZH}$ | GND | | |

**Figure 2. Test Circuit**

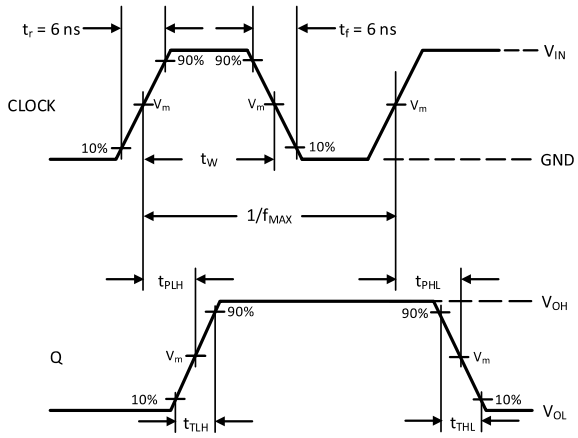



**Figure 3.**

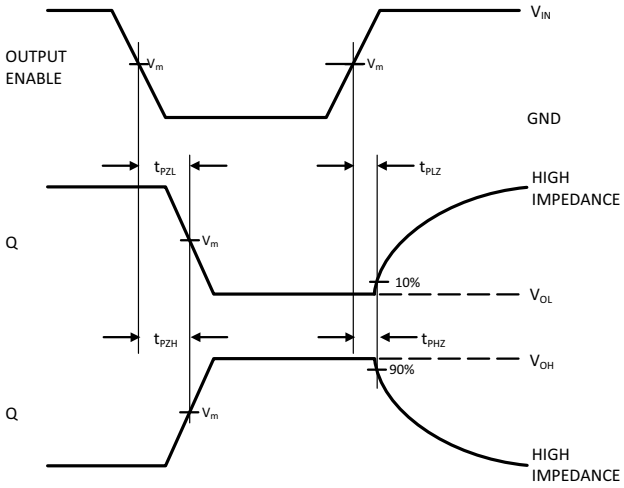



**Figure 4.**

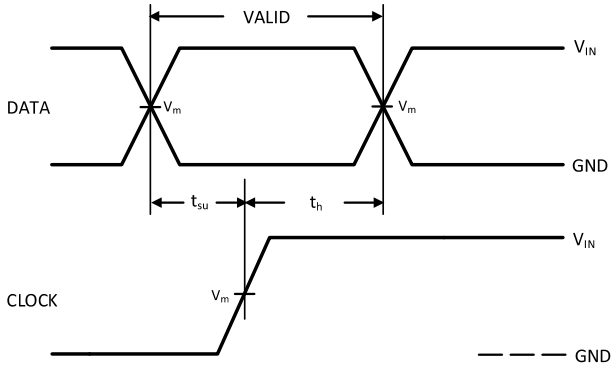



**Figure 5.**

| Device | $V_{IN}$, V | $V_m$, V |
|---|---|---|
| MC74HC374A | $V_{CC}$ | 50% x $V_{CC}$ |
| MC74HCT374A | 3 V | 1.3 V |

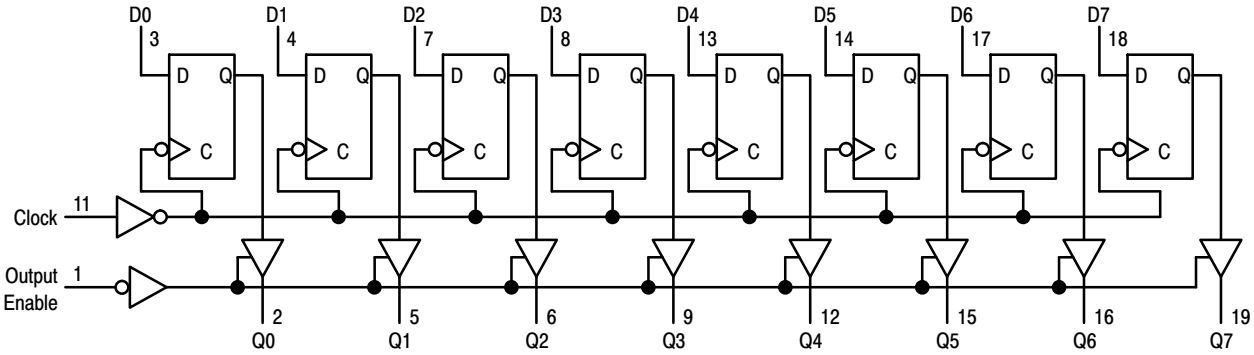



**Figure 6. Expanded Logic Diagram**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MC74HC374ADWG | HC374A | SOIC−20 Wide | 38 Units / Rail |
| MC74HC374ADWR2G | HC374A | SOIC−20 Wide | 1000 / Tape & Reel |
| MC74HC374ADWR2G−Q* | HC374A | SOIC−20 Wide | 1000 / Tape & Reel |
| MC74HC374ADTR2G | HC<br>374A | TSSOP−20 | 2500 / Tape & Reel |
| MC74HC374ADTR2G−Q* | HC<br>374A | TSSOP−20 | 2500 / Tape & Reel |
| MC74HCT374ADWG | HCT374A | SOIC−20 Wide | 38 Units / Rail |
| MC74HCT374ADWR2G | HCT374A | SOIC−20 Wide | 1000 / Tape & Reel |
| MC74HCT374ADWR2G−Q* | HCT374A | SOIC−20 Wide | 1000 / Tape & Reel |
| MC74HCT374ADTR2G | HCT<br>374A | TSSOP−20 | 2500 / Tape & Reel |
| MC74HCT374ADTR2G−Q* | HCT<br>374A | TSSOP−20 | 2500 / Tape & Reel |

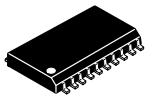
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

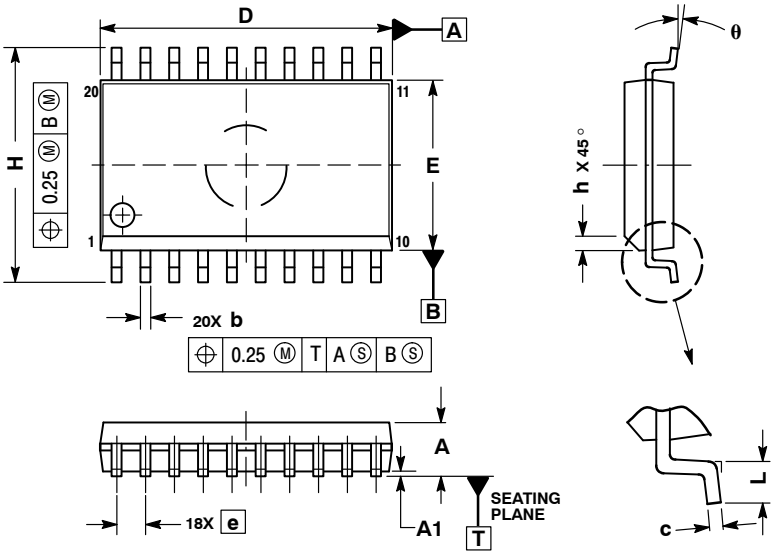
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



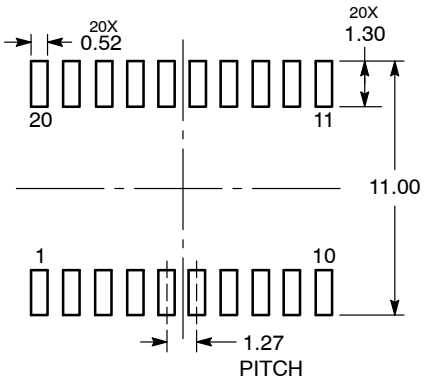
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

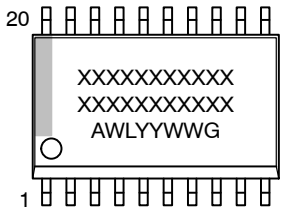
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC−20 WB** | **PAGE 1 OF 1** |

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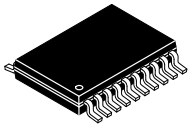
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

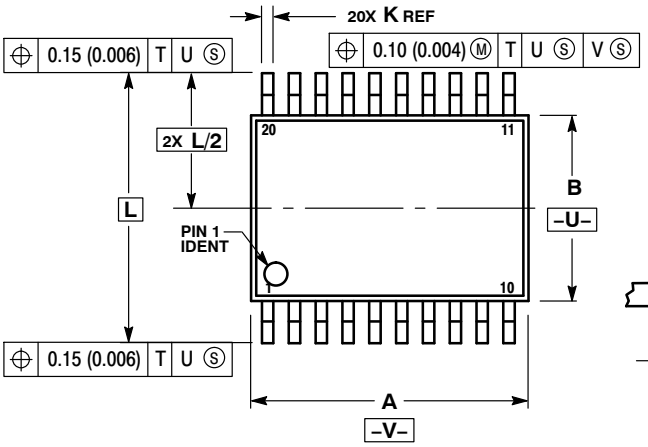
ON Semiconductor®

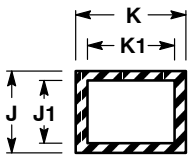
**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016

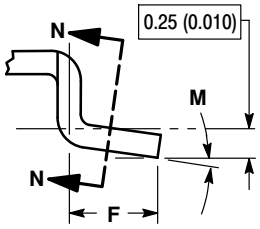


SCALE 2:1

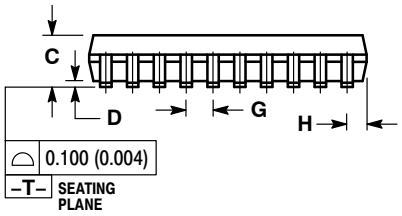


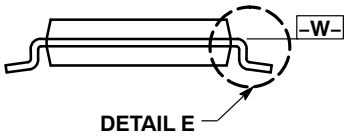




SECTION N−N




DETAIL E

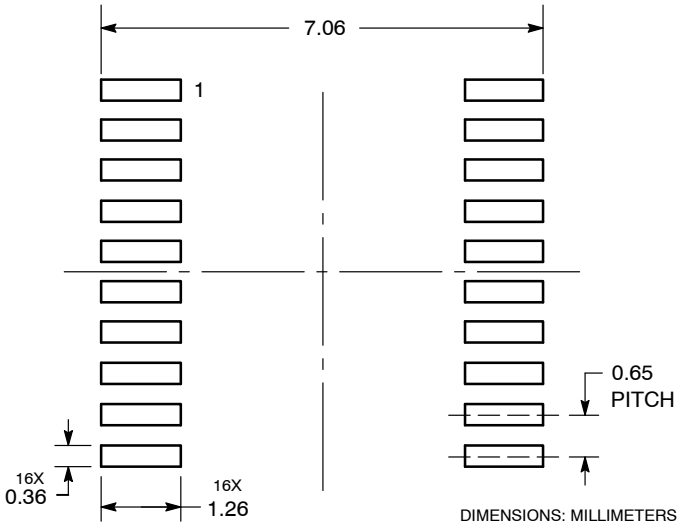



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

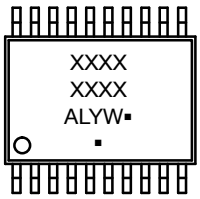
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
| DESCRIPTION: | TSSOP−20 WB | PAGE 1 OF 1 |

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