

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

High-Performance Silicon-Gate CMOS

MC74HC589A

The MC74HC589A device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see the Function Table). The shift register output, Q_H , is a 3-state output, allowing this device to be used in bus-oriented systems.

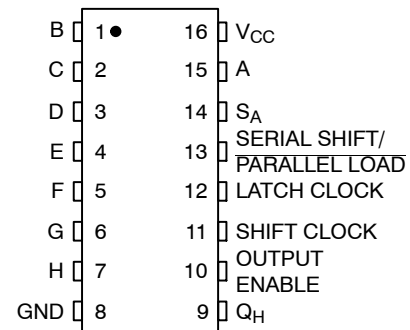
The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

Features

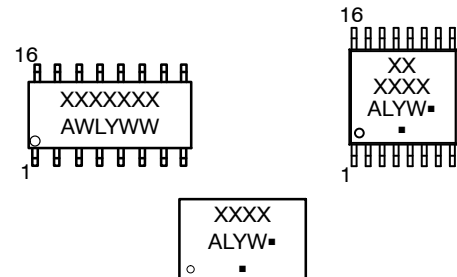
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



PIN ASSIGNMENT



MARKING DIAGRAMS



- A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

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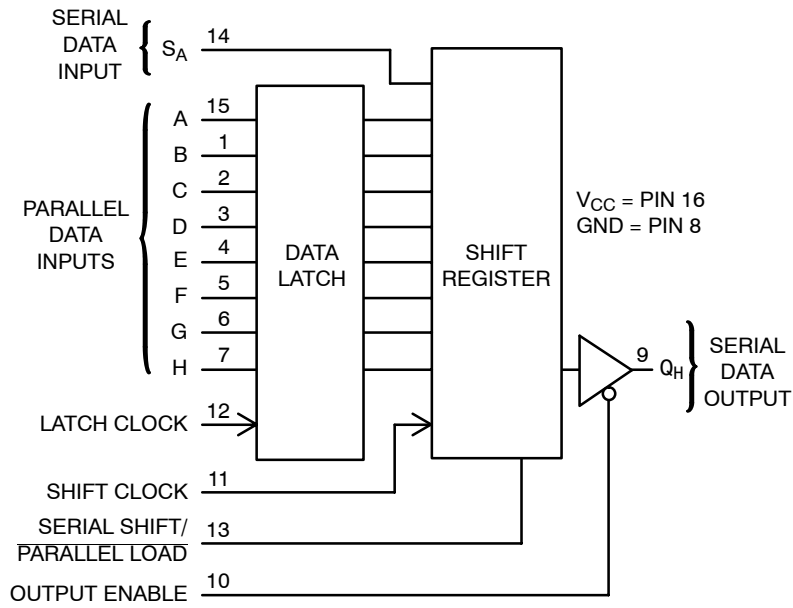


Figure 1. Logic Diagram

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S _A	Parallel Inputs A-H	Data Latch Contents	Shift Register Contents	Output Q _H
Force Output into High Impedance State	H	X			X	X	X	X	Z X
Load Parallel Data into Data Latch	L	H	↗	L, H, ↘	X	a-h	a-h	U	U
Transfer Latch Contents to Shift Register	L	L	L, H, ↘	X	X	X	U	LR _N → SR _N	LR _H
Contents of Input Latch and Shift Register are Unchanged	L	H	L, H, ↘	L, H, ↘	X	X	U	U	U
Load Parallel Data into Data Latch and Shift Register	L	L	↗		X	a-h	a-h	a-h	h X
Shift Serial Data into Shift Register	L	H		↗	D	X	*	SR _A = D, SR _N → SR _{N+1}	SR _G → SR _H
Load Parallel Data in Data Latch and Shift Serial Data into Shift Register	L	H	↗	↗	D	a-h	a-h	SR _A = D, SR _N → SR _{N+1}	SR _G → SR _H

LR	=	latch register contents	U	=	remains unchanged
SR	=	shift register contents	X	=	don't care
a-h	=	data at parallel data inputs A-H	Z	=	high impedance
D	=	data (L, H) at serial data input S _A	*	=	depends on Latch Clock input

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V
V _{IN}	DC Input Voltage	−0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage	−0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Diode Current, per Pin	±20	mA
I _{OUT}	DC Input Diode Current, Per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	±20	mA
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	±20	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 1) SOIC−16126 QFN16118 TSSOP−16159		°C/W
P _D	Power Dissipation in Still Air at 25°C SOIC−16995 QFN161062 TSSOP−16787		mW
MSL	Moisture Sensitivity	Level 1	–
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 2) Human Body Model> 4000 Charged Device ModelN/A		V
I _{LATCHUP}	Latchup Performance (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 3)	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC}	Guaranteed Limit			Unit
			V	-55°C to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	2.48	2.34	2.20	
		I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.70	
		I _{out} ≤ 7.8 mA	6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	0.26	0.33	0.40	
		I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.40	
		I _{out} ≤ 7.8 mA	6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC}	Guaranteed Limit			Unit
		V	–55°C to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 2 and 3)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 4)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 2 and 6)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _H (Figures 2 and 5)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _H (Figures 2 and 5)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
C _{in}	Maximum Input Capacitance	–	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		50	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

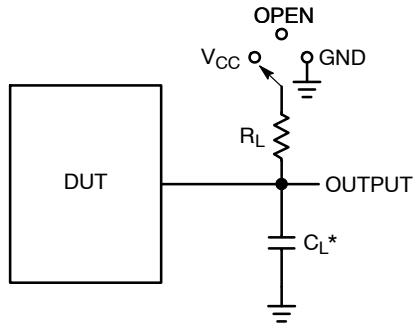
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TIMING REQUIREMENTS

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤85°C	≤125°C	
t _{su}	Minimum Setup Time, A-H to Latch Clock (Figure 7)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Data Input S _A to Shift Clock (Figure 8)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 9)	2.0	100	125	150	ns
		3.0	40	50	60	
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Latch Clock to A-H (Figure 7)	2.0	25	30	40	ns
		3.0	10	12	15	
		4.5	5	6	8	
		6.0	5	6	7	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input S _A (Figure 8)	2.0	5	5	5	ns
		3.0	5	5	5	
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Shift Clock (Figure 4)	2.0	75	95	110	ns
		3.0	40	50	60	
		4.5	15	19	23	
		6.0	13	16	19	
t _w	Minimum Pulse Width, Latch Clock (Figure 3)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 6)	2.0	80	100	120	ns
		3.0	40	50	60	
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

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SWITCHING WAVEFORMS



*C_L Includes probe and jig capacitance

Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 2. Test Circuit

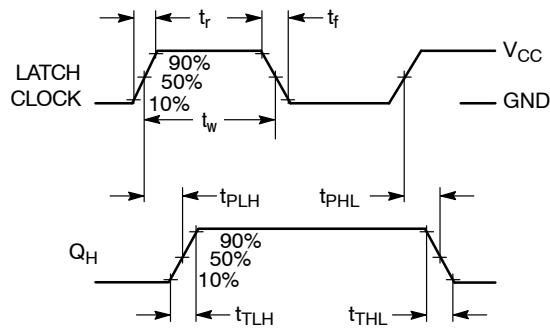


Figure 3. (Serial Shift/Parallel Load = L)

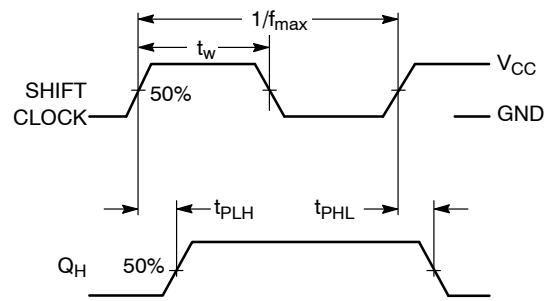


Figure 4. (Serial Shift/Parallel Load = H)

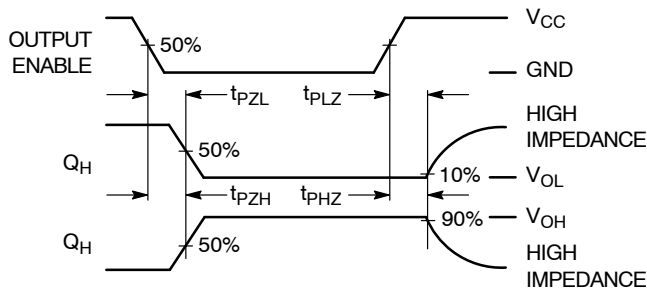


Figure 5.

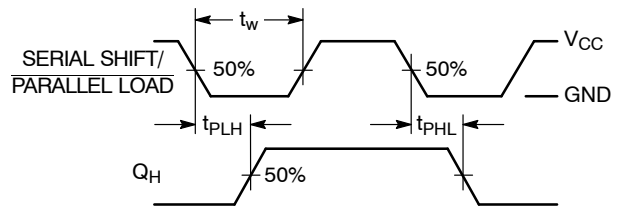


Figure 6.

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SWITCHING WAVEFORMS

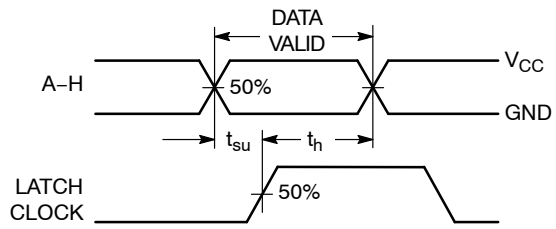


Figure 7.

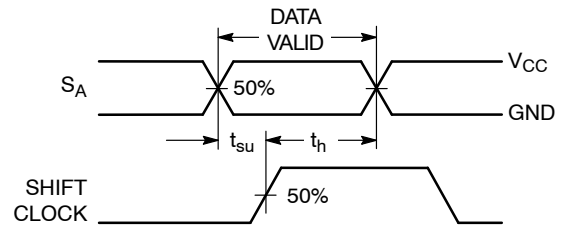


Figure 8.

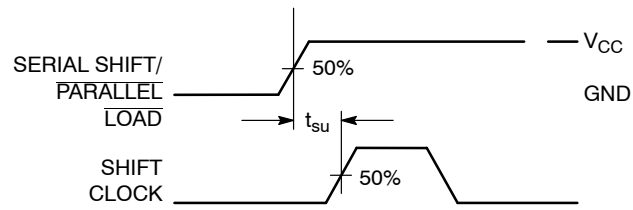


Figure 9.

PIN DESCRIPTIONS**DATA INPUTS****A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)**

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS**Serial Shift/Parallel Load (Pin 13)**

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and

data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low-to-high transition on this input loads the parallel data on inputs A–H into the data latch.

Output Enable (Pin 10)

Active-low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

OUTPUT**Q_H (Pin 9)**

Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.

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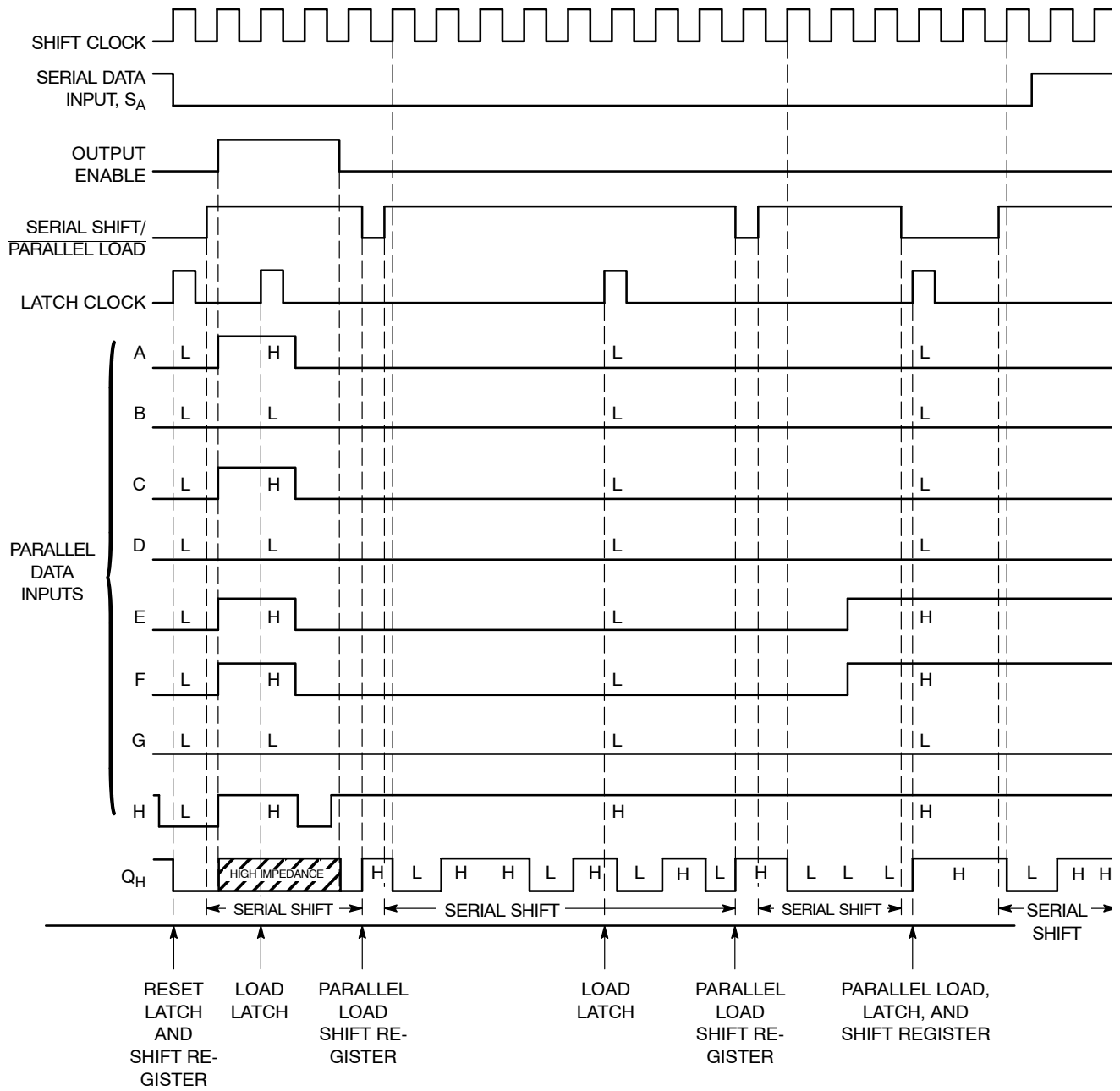


Figure 10. Timing Diagram

MC74HC589A

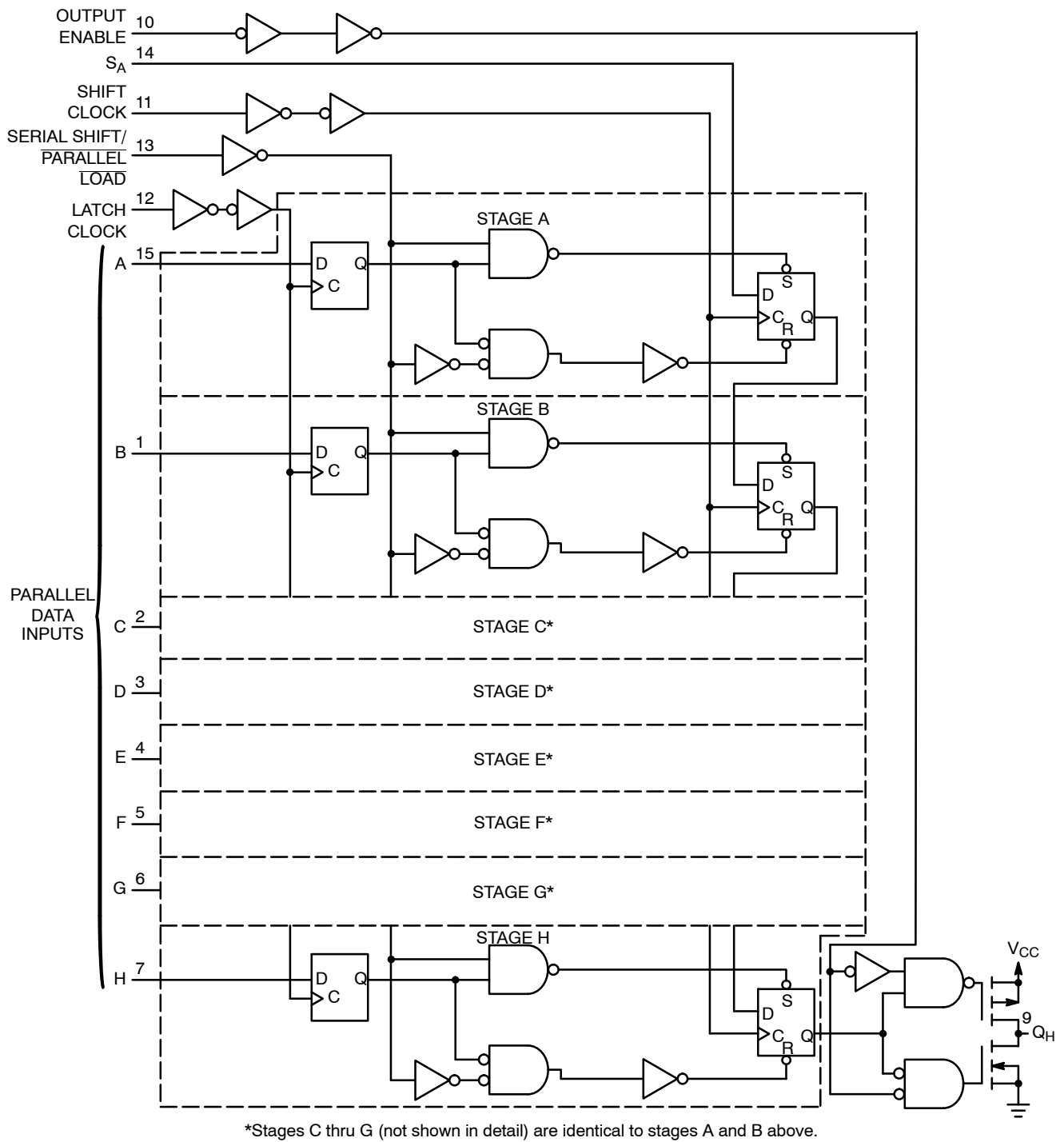


Figure 11. Logic Detail

MC74HC589A

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC589ADG	HC589AG	SOIC-16	48 Units / Rail
MC74HC589ADR2G	HC589AG	SOIC-16	2500 / Tape & Reel
MC74HC589ADR2G-Q*	HC589AG	SOIC-16	2500 / Tape & Reel
MC74HC589ADTR2G	HC 589A	TSSOP-16	2500 / Tape & Reel
MC74HC589ADTR2G-Q*	HC 589A	TSSOP-16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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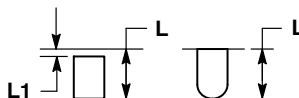
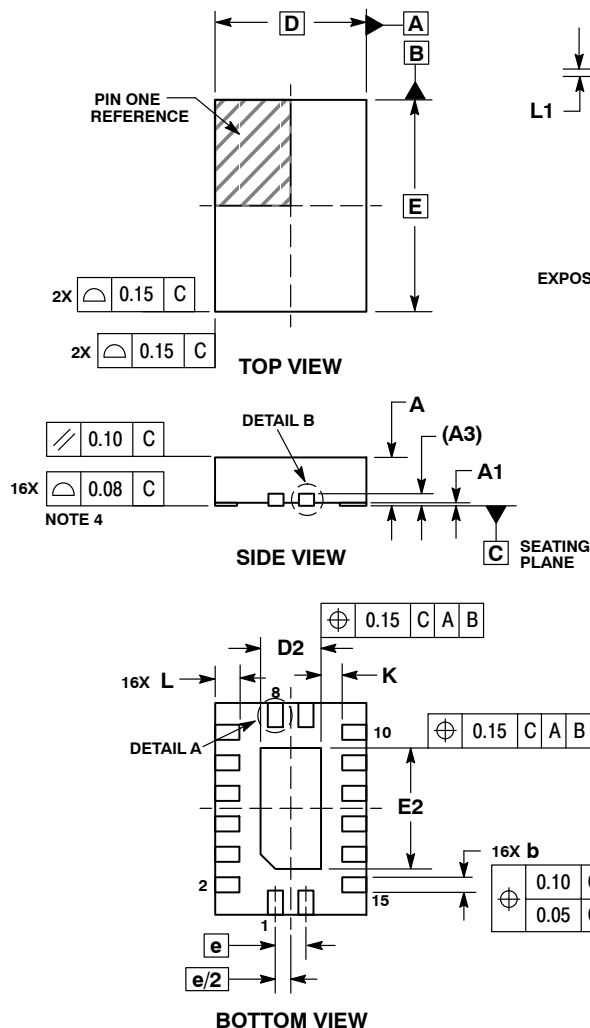
PACKAGE DIMENSIONS



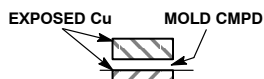
SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

DATE 11 DEC 2008



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



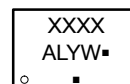
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.50	BSC
D2	0.85	1.15
E	3.50	BSC
E2	1.85	2.15
e	0.50	BSC
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

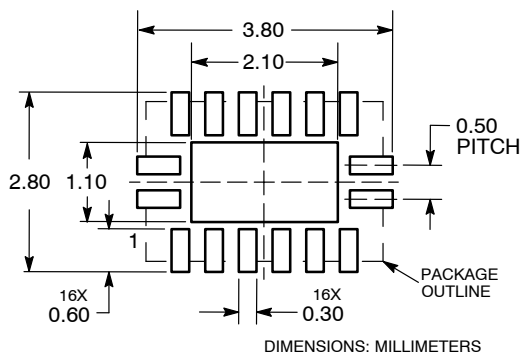


- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

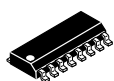
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



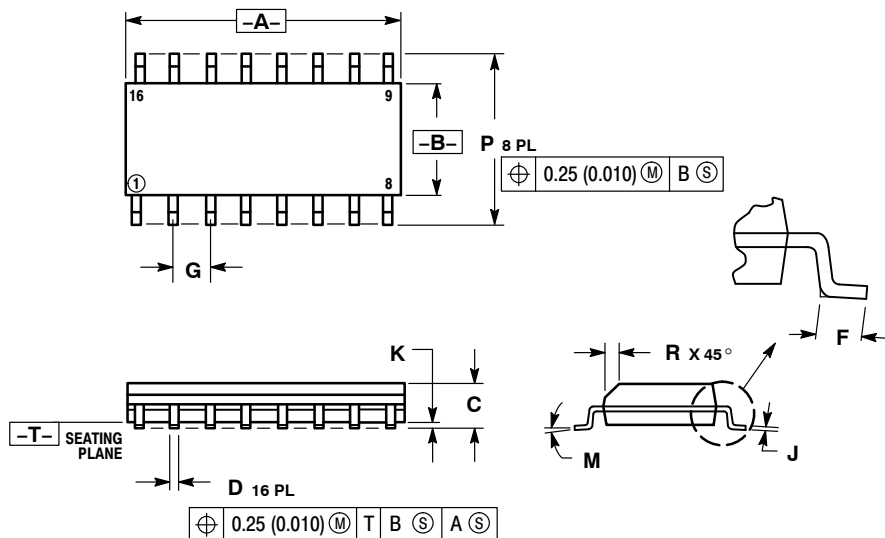
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SOIC-16

CASE 751B-05

ISSUE K

DATE 29 DEC 2006



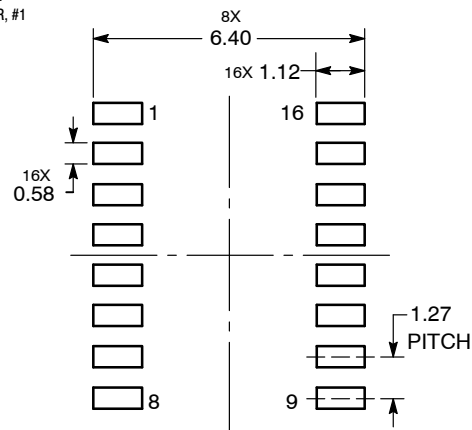
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

RECOMMENDED SOLDERING FOOTPRINT*



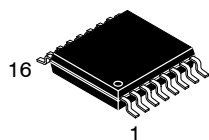
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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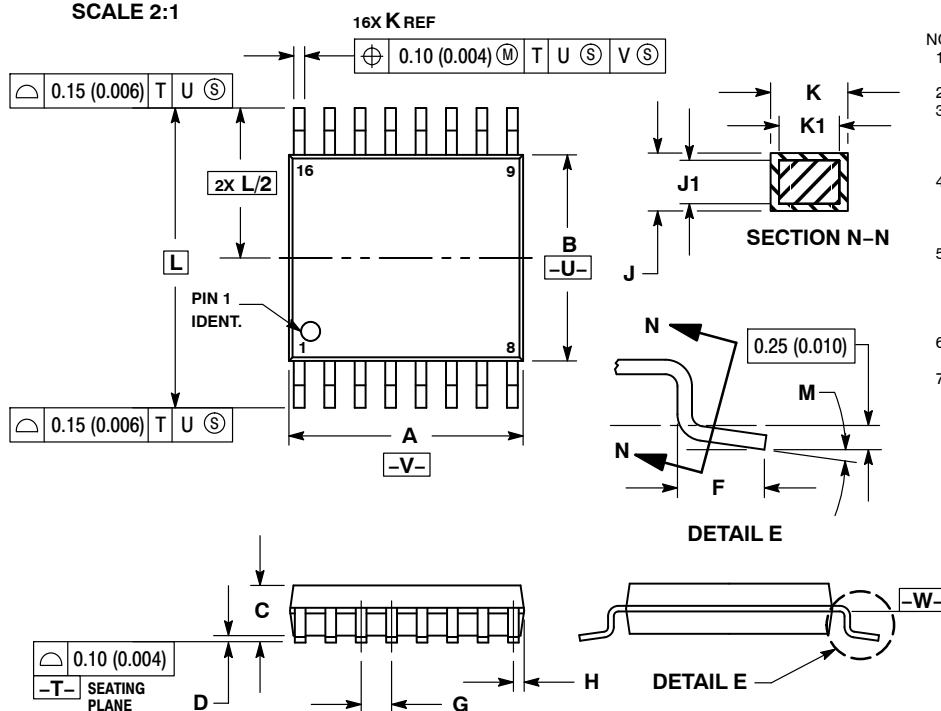
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

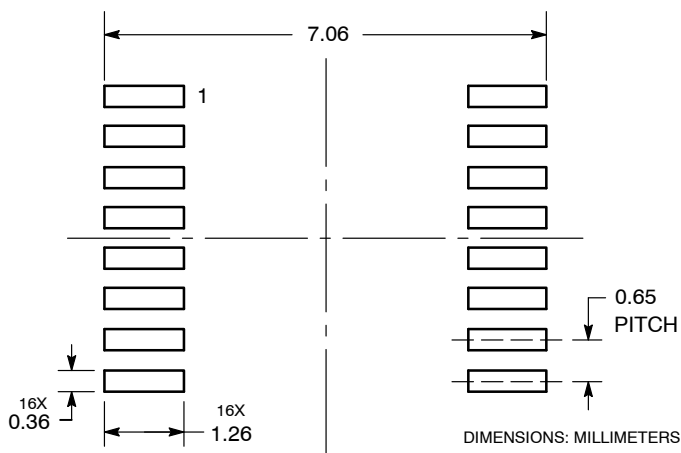


NOTES:

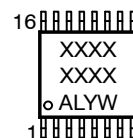
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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