

Automotive Gate Driver IC, High and Low Side

600 V, 4.5 A

FAN7191-F085, FAD7191

Description

The FAN7191 / FAD7191 is a monolithic high- and low-side gate-driver IC, which can drive high speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse driving capability and minimum cross-conduction.

ON Semiconductor's high-voltage process and common-mode noise canceling technique provide stable operation of high-drivers under high dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V.

The UVLO circuit prevents malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

The high current and low output voltage drop features make this device suitable for controlling direct injection actuators and for use in many automotive DC-DC converter and motor control applications.

Features

- Floating Channel for Bootstrap Operation to +600 V
- 4.5 A Sourcing and 4.5 A Sinking Current Driving Capability
- Common-Mode dV/dt Noise Cancelling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- Output In-phase with Input
- Enable Pin (For 14-SOP Package Only)
- 14-SOP with Separate Signal and Power Ground for Enhanced Noise Immunity
- 14-SOP with Increased Clearance for High Voltage Applications
- Automotive Applications, AEC Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Electric and Hybrid Electric Vehicles
- 48 V Mild Hybrid Vehicles
- Automotive High Voltage DC-DC converters
- Motor Control (Fans, Pumps, Compressors)
- Advanced Fuel Injection Systems
- Starter/Alternator
- Electric Power Steering
- MOSFET and IGBT Driver Applications



SOIC8
CASE 751EB



SOIC14
CASE 751EF

ORDERING INFORMATION

Part Number	Package	Shipping [†]
FAN7191MX-F085	8-SOP (751EB)	2500 / Tape & Reel
FAN7191MX-F085-1	8-SOP (751EB)	
FAD7191M1X	14-SOP (751EF)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Application Circuit

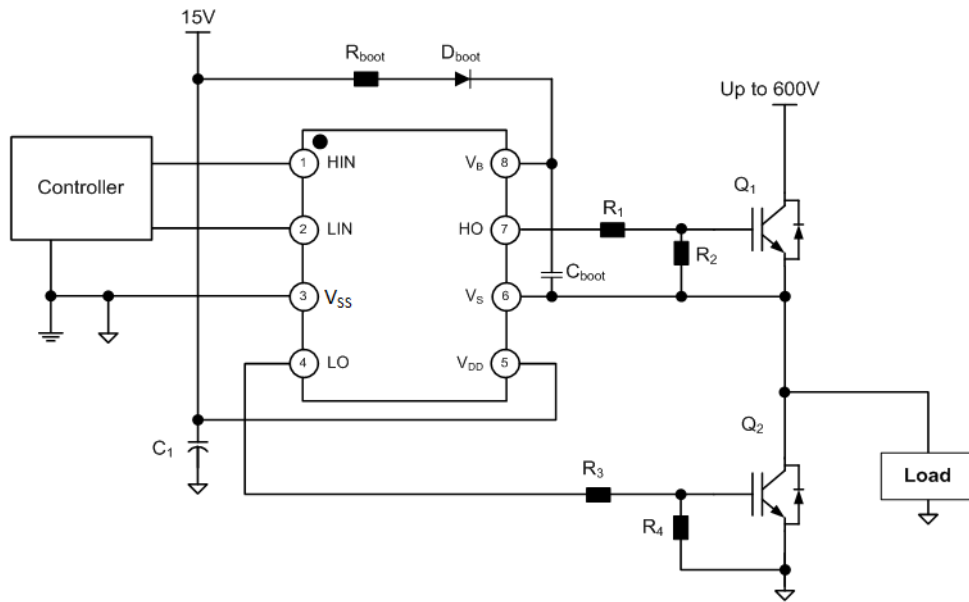


Figure 1. Half-Bridge Application Circuit (8-SOP)

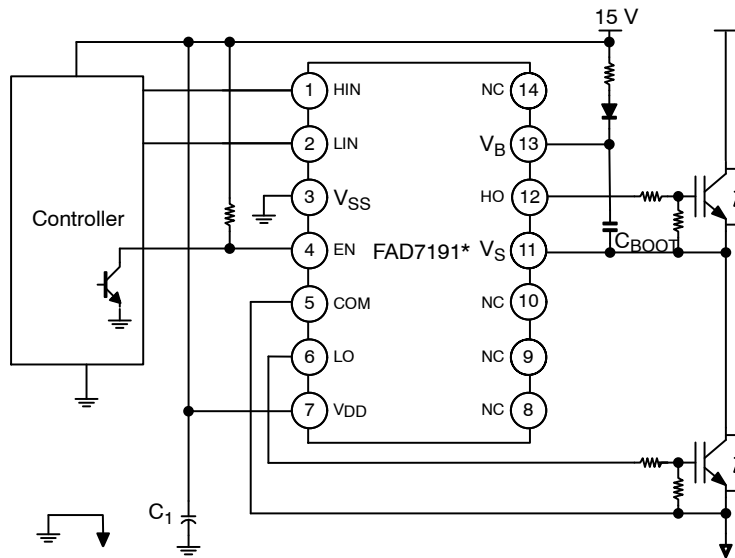


Figure 2. Half-Bridge Application Circuit (14-SOP)

FAN7191-F085, FAD7191

INTERNAL BLOCK DIAGRAM

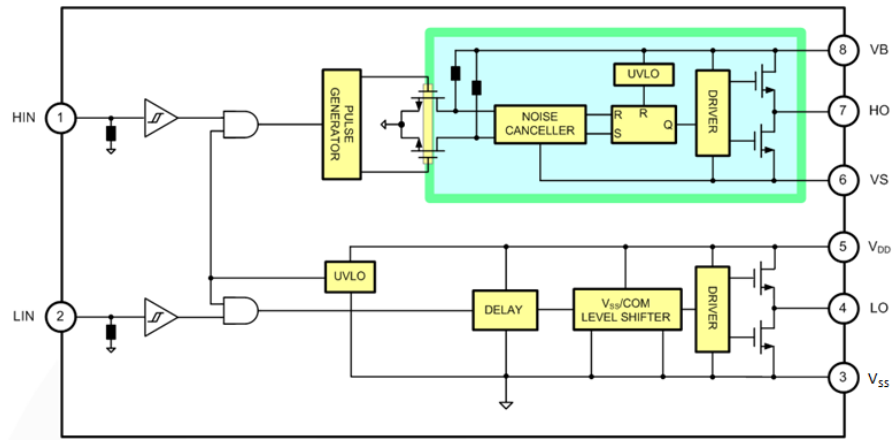


Figure 3. Functional Block Diagram (8-SOP)

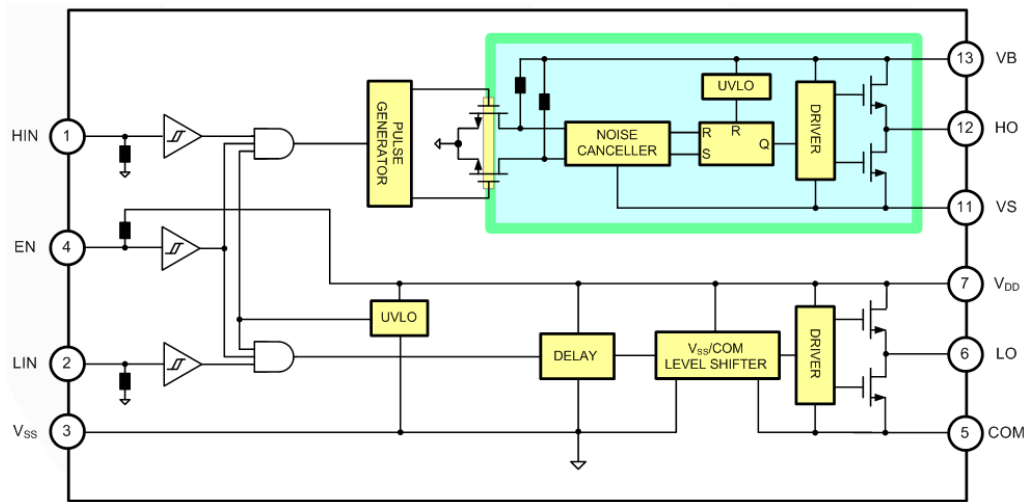


Figure 4. Functional Block Diagram (14-SOP)

FAN7191–F085, FAD7191

Pin Assignment

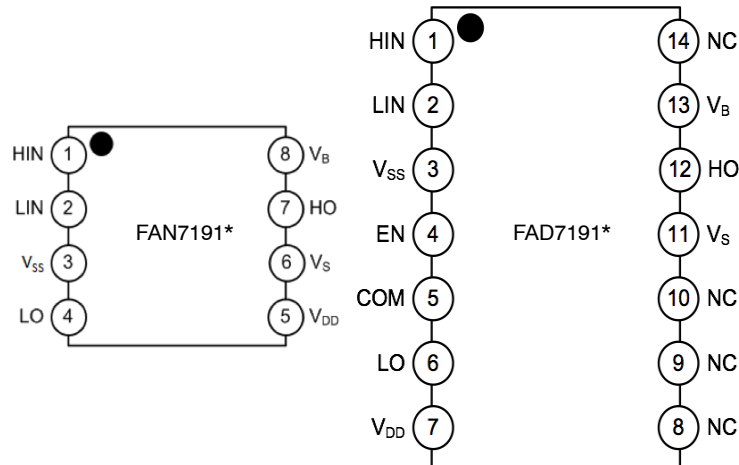


Figure 5. Pin Assignments (Top View)

Table 1. PIN DEFINITIONS

8–Pin	14–Pin	Name	Description
1	1	HIN	Logic Input for High–Side Gate Driver Output
2	2	LIN	Logic Input for Low–Side Gate Driver Output
3	3	V _{SS}	Logic Ground, Power ground for 8–SOP
	4	EN	Enable Input (Internal Pull Up)
	5	COM	Power Ground for 14–SOP, Low–side Driver Return
4	6	LO	Low–Side Driver Output
5	7	V _{DD}	Low–Side and Logic Power Supply Voltage
6	11	V _S	High–Side Floating Supply Return
7	12	HO	High–Side Driver Output
8	13	V _B	High–Side Floating Supply
	8, 9, 10, 14	NC	No Connect

FAN7191–F085, FAD7191

Table 2. ABSOLUTE MAXIMUM RATINGS

($T_A = -40^{\circ}\text{C}$ to 125°C , unless otherwise specified. V_B , V_{DD} and V_{IN} are referenced to V_{SS})

Symbol	Parameter		Min.	Max.	Unit
V_S	High-side offset voltage V_S		$V_B - 25$	$V_B + 0.3$	V
V_B	High-side floating supply voltage V_B		-0.3	625	V
V_{HO}	High-side floating output voltage		$V_S - 0.3$	$V_B + 0.3$	V
V_{DD}	Low-side and logic-fixed supply voltage		-0.3	25	V
COM	Power Ground (14-SOP)		$V_{DD} - 25$	$V_{DD} + 0.3$	V
V_{IN}	Logic Input voltage (HIN, LIN, EN)		-0.3	$V_{DD} + 0.3$	V
V_{LO}	Low-Side Output Voltage LO (8-SOP)		$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Low-Side Output Voltage LO (14-SOP)		COM - 0.3	$V_{DD} + 0.3$	V
T_{pulse} (Note 4)	Minimum Pulse Width		80		ns
dV_S/dt	Allowable offset voltage slew rate			50	V/ns
P_D (Note 1, 2, 3)	Power Dissipation, $T_A = 25^{\circ}\text{C}$	8-SOP		0.625	W
		14-SOP		0.80	W
θ_{JA} (Note 1, 2)	Thermal Resistance, junction-to-ambient	8-SOP		200	$^{\circ}\text{C/W}$
		14-SOP		156	$^{\circ}\text{C/W}$
T_J	Junction temperature			+150	$^{\circ}\text{C}$
T_S	Storage temperature		-55	+150	$^{\circ}\text{C}$
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8-SOP	2500	V
			14-SOP	2000	
		Charged Device Model, JESD22-C101		2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on $76.2 \times 114.3 \times 1.6$ mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards: JESD51-2: Integral circuits thermal test method environmental conditions – natural convection. JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
3. P_D is the power that raises T_J to 150°C for $T_A = 25^{\circ}\text{C}$. P_D to be derated at higher ambient temperature.
4. Minimum input pulse width that guarantee to produce an output pulse. Valid for turn on and turn off pulse width.

Table 3. RECOMMENDED OPERATING CONDITIONS (V_S , V_{DD} and V_{IN} are referenced to V_{SS})

Symbol	Parameter	Min.	Max.	Unit
V_B	High-side floating supply voltage	$V_S + 10$	$V_S + 22$	V
V_S	High-side Floating Supply Offset Voltage	$6 - V_{BS}$	600	V
V_{HO}	High-side Output Voltage	V_S	V_B	V
V_{DD}	Low-side and Logic Supply voltage	10	22	V
V_{LO}	Low-side output voltage (8-SOP)	0	V_{DD}	V
	Low-side output voltage (14-SOP)	COM	V_{DD}	V
V_{IN}	Logic input voltage (HIN, LIN, EN)	0	V_{DD}	V
COM	Power Ground (14-SOP)	$V_{DD} - 22$	V_{DD}	V
T_A	Ambient Temperature	-40	+125	$^{\circ}\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD} , V_{BS}) = 15.0 V, $V_S = V_{SS} = \text{COM}$, $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input signals HIN and LIN. The V_O and I_O parameters are referenced to COM (or V_{SS} in case of 8–SOP). V_S and COM (V_{SS} for 8–SOP) are applicable to the respective outputs HO and LO)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY SECTION (V _{DD} AND V _{BS})						
V _{DDUV+} V _{BSUV+}	V _{DD} and V _{BS} Supply Under-Voltage Positive-going Threshold		7.8	8.8	9.8	V
V _{DDUV-} V _{BSUV-}	V _{DD} and V _{BS} Supply Under-Voltage Negative Going Threshold		7.2	8.3	9.1	
V _{DDHYS}	V _{DD} supply under-voltage lockout hysteresis			0.5		
I _{LK}	Offset Supply Leakage Current	V _B = V _S = 600 V			50	μA
I _{QBS}	Quiescent V _{BS} Supply Current	V _{IN} = 0 V or 5 V		45	110	
I _{QDD}	Quiescent V _{DD} Supply Current	V _{IN} = 0 V or 5 V		75	150	
I _{PBS}	Operating V _{BS} Supply Current	f _{IN} = 20 kHz, RMS value (See Figure 26)		400	800	μA
I _{PDD}	Operating V _{DD} Supply Current	f _{IN} = 20 kHz, RMS value (See Figure 26)		400	800	
LOGIC INPUT SECTION (H _{IN} , L _{IN} , E _N)						
V _{IH}	Logic “1” Input Voltage		2.5			V
V _{IL}	Logic “0” Input Voltage				1.2	
I _{IN+}	Logic “1” Input Bias Current (H _{IN} /L _{IN})	V _{IN} = 5 V		25	50	μA
I _{IN-}	Logic “0” Input Bias Current (H _{IN} /L _{IN})	V _{IN} = 0 V		1.0	2.0	
I _{EN+}	Enable High Input Bias Current	E _N = 5 V	–100	–50	–10	
I _{EN-}	Enable Low Input Bias Current	E _N = 0 V	–140	–75	–20	
R _{IN}	Input Pull-down Resistance		100	200		kΩ
GATE DRIVER OUTPUT SECTION (H _O , L _O)						
V _{OH}	High-level Output Voltage, V _{BIAS} –V _O	No Load			1.35	V
V _{OL}	Low-level Output Voltage, V _O	No Load			35	mV
I _{O+} (Note 5)	Output HIGH, Short-circuit Pulsed Current	V _O = 0 V, V _{IN} = 5 V with PW < 10μs	3.5	4.5		A
I _{O-} (Note 5)	Output LOW Short-circuit Pulsed Current	V _O = 15 V, V _{IN} = 0 V with PW < 10 μs	3.5	4.5		
V _S	Allowable Negative V _S Pin Voltage for H _{IN} Signal Propagation to H _O	V _{BS} = 15V		–9.8	–9.0	V
COM–V _{SS} (Note 5)	Allowable COM–V _{SS} ground offset	14–SOP, V _{DD} = 15 V, V _{SS} = 0 V	–7.0			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Parameters guaranteed by design.

FAN7191–F085, FAD7191

Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD} , V_{BS}) = 15.0 V, $V_S = V_{SS} = COM = 0$ V, $T_A = -40^{\circ}C$ to $125^{\circ}C$, $C_{LOAD} = 1000$ pF unless otherwise specified)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Propagation Delay	$V_S = 0$ V		140	200	ns
t_{off}	Turn-off Propagation Delay	$V_S = 0$ V		140	200	ns
MT	Delay Matching				55	ns
t_r	Turn-on Rise Time			25	50	ns
t_f	Turn-off Fall Time			25	50	ns

Typical Characteristics

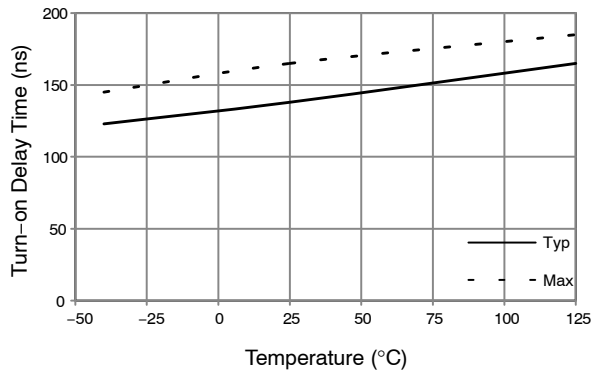


Figure 6. Turn-on Propagation Delay vs. Temperature

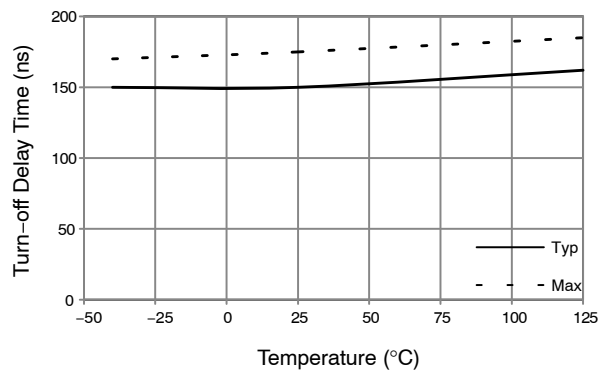


Figure 7. Turn-off Propagation Delay vs. Temperature

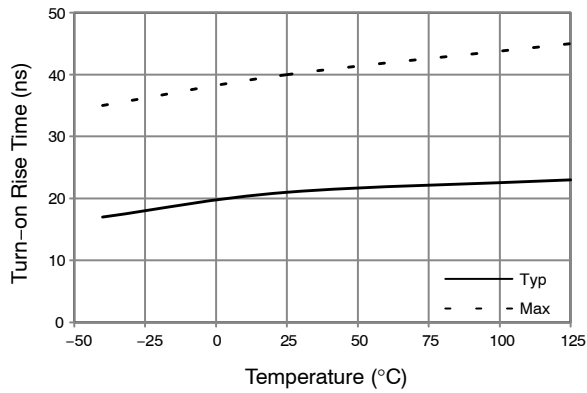


Figure 8. Turn-on Rise Time vs. Temperature

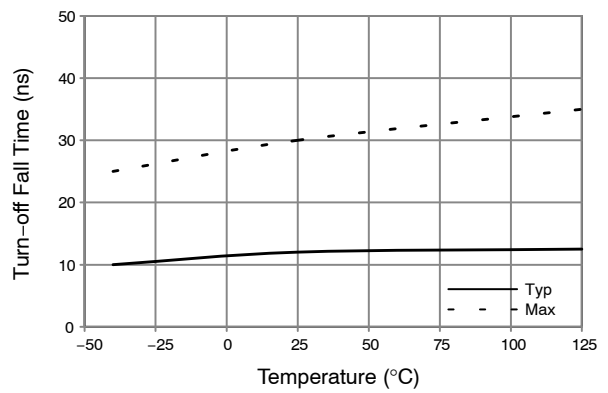


Figure 9. Turn-off Fall Time vs. Temperature

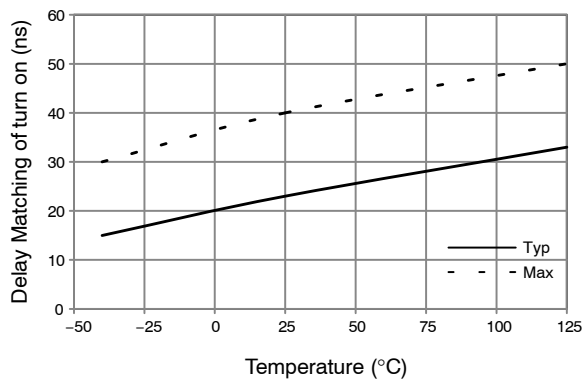


Figure 10. Turn-on Delay Matching vs. Temperature

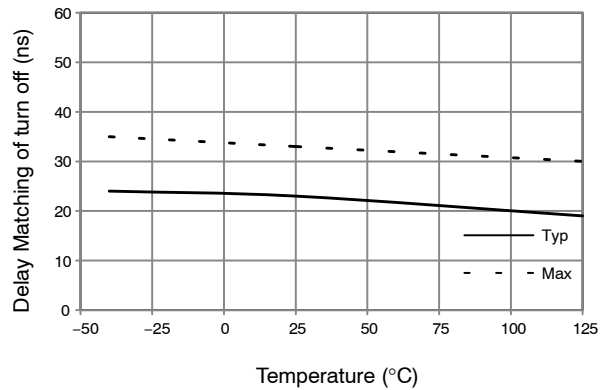


Figure 11. Turn-off Delay Matching vs. Temperature

Typical Characteristics (continued)

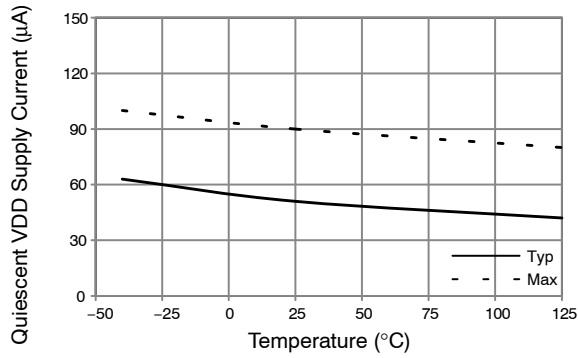


Figure 12. Quiescent V_{DD} Supply Current vs. Temperature

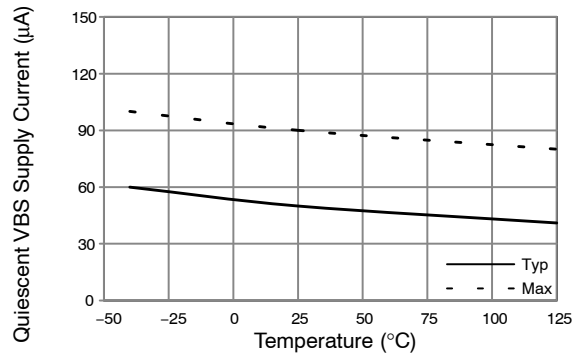


Figure 13. Quiescent V_{BS} Supply Current vs. Temperature

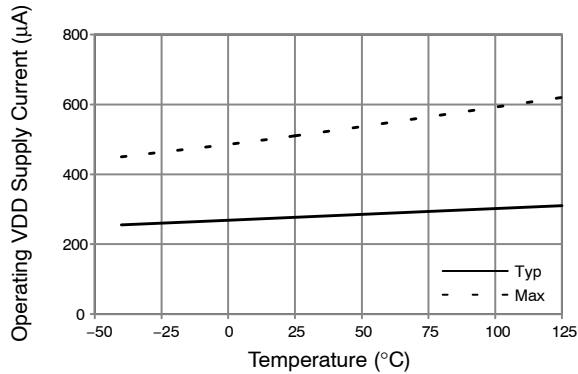


Figure 14. Operating V_{DD} Supply Current vs. Temperature

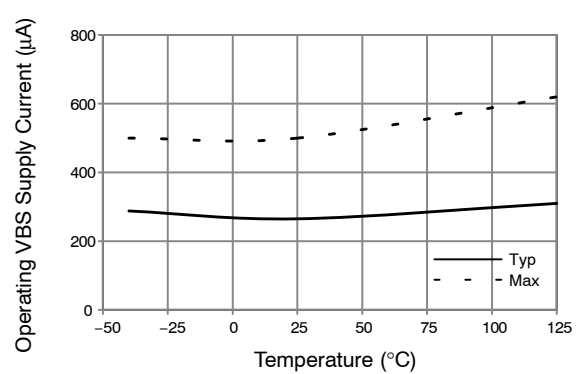


Figure 15. Operating V_{BS} Supply Current vs. Temperature

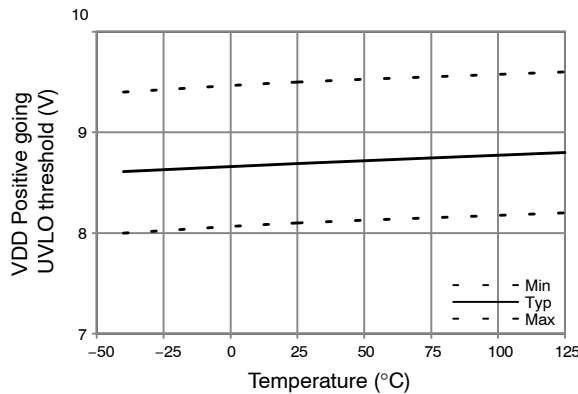


Figure 16. V_{DD} UVLO+ vs. Temperature

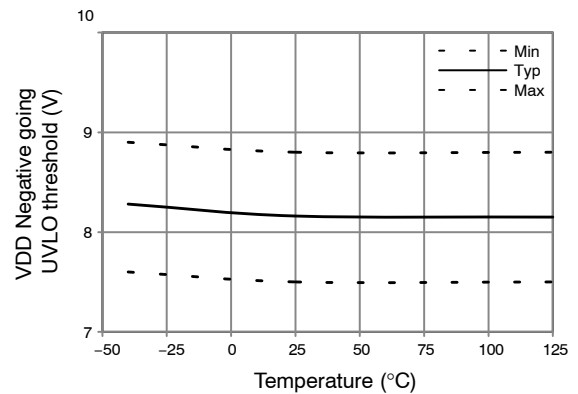


Figure 17. V_{DD} UVLO- vs. Temperature

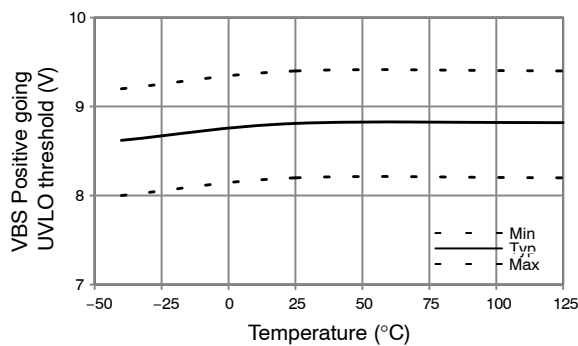


Figure 18. V_{BS} UVLO+ vs. Temperature

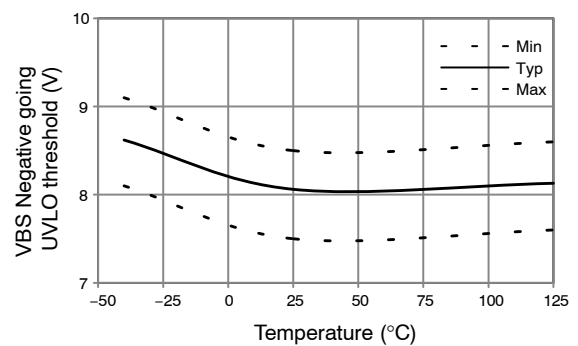


Figure 19. V_{BS} UVLO- vs. Temperature

Typical Characteristics (continued)

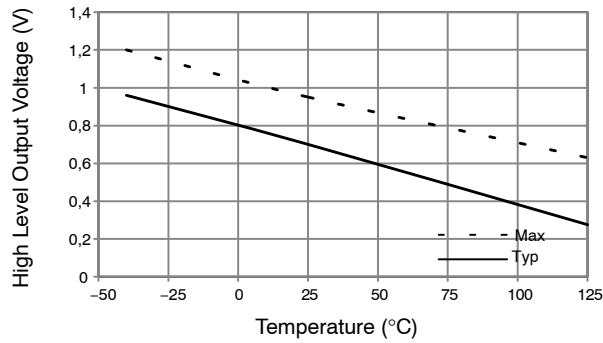


Figure 20. High-Level Output Voltage vs. Temperature

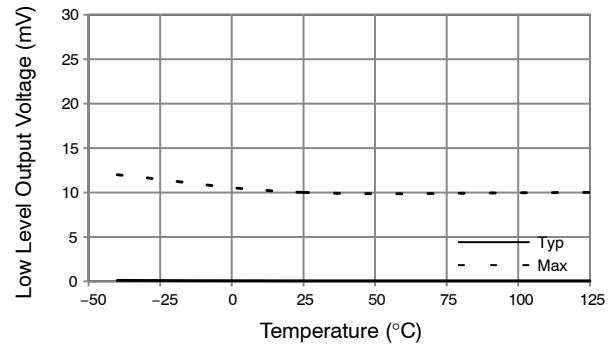


Figure 21. Low-Level Output Voltage vs. Temperature

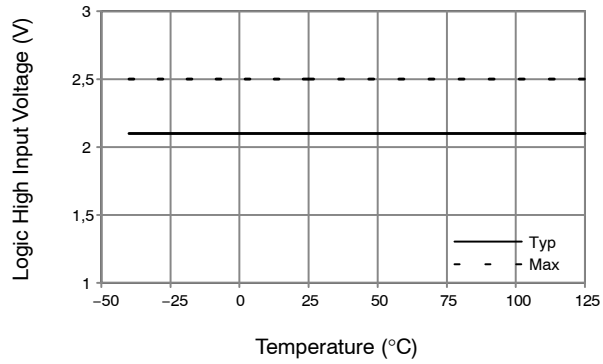


Figure 22. Logic High Input Voltage vs. Temperature

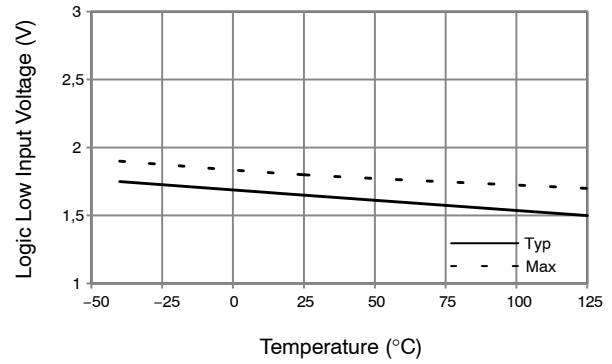


Figure 23. Logic Low Input Voltage vs. Temperature

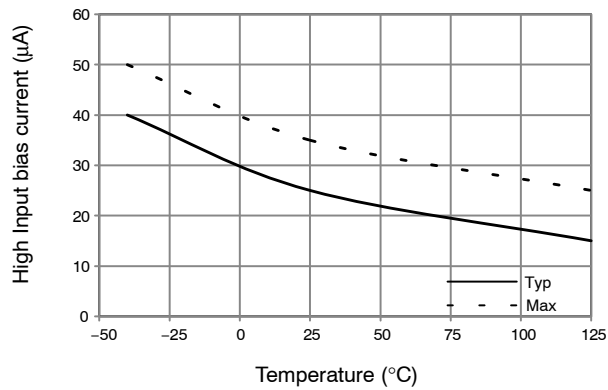


Figure 24. Logic "1" Input Bias Current vs. Temperature

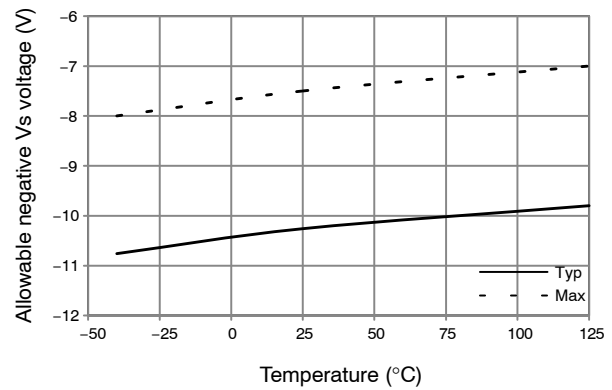


Figure 25. Allowable Negative VS Voltage vs. Temperature

Switching Time Definitions

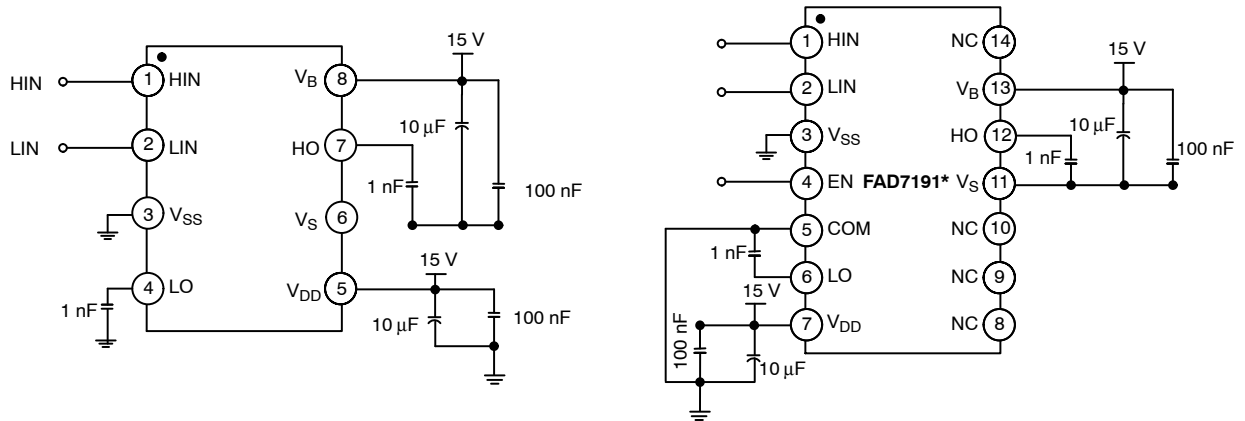


Figure 26. Switching Time Test Circuit

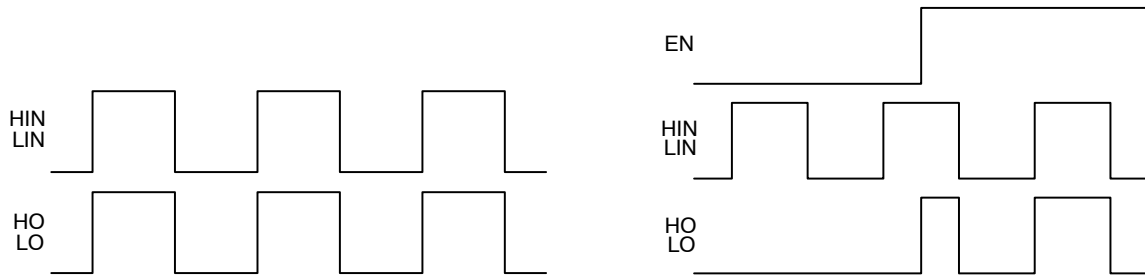


Figure 27. Input / Output Timing Diagram

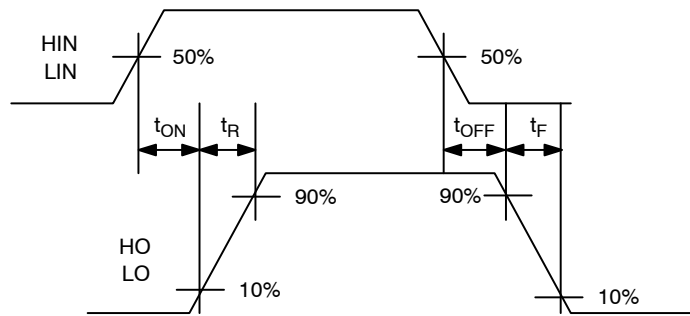


Figure 28. Switching Time Waveform Definitions

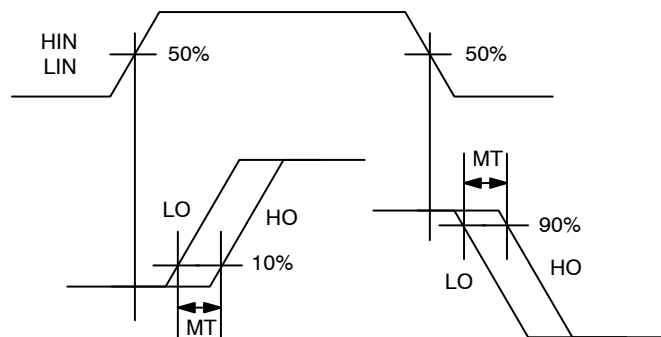


Figure 29. Delay Matching Waveform Definition

MECHANICAL CASE OUTLINE

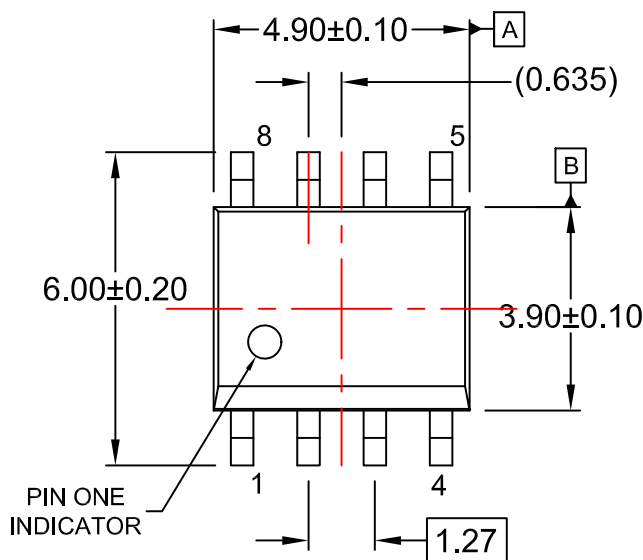
PACKAGE DIMENSIONS

ON Semiconductor®

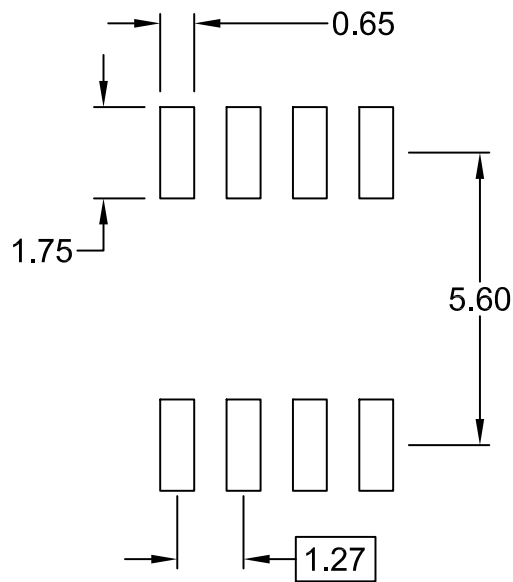


SOIC8
CASE 751EB
ISSUE A

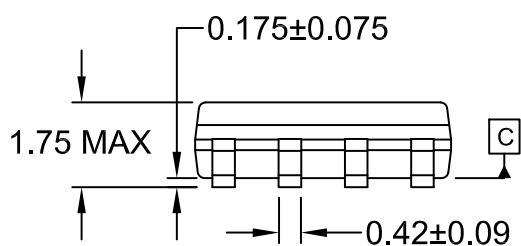
DATE 24 AUG 2017



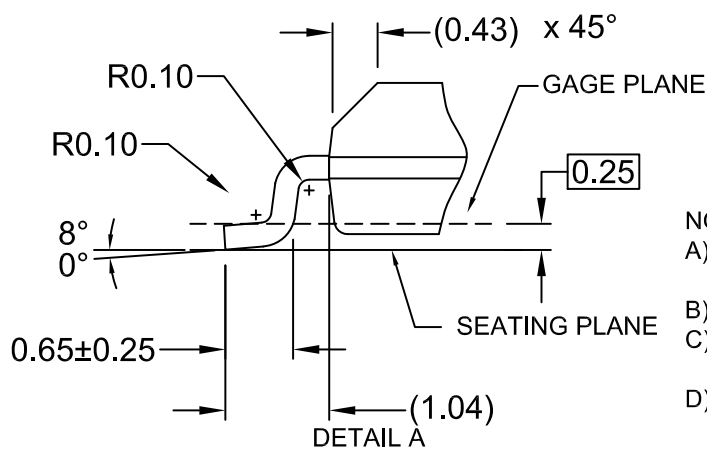
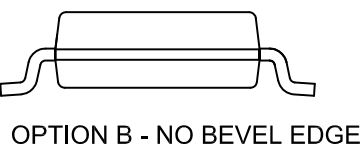
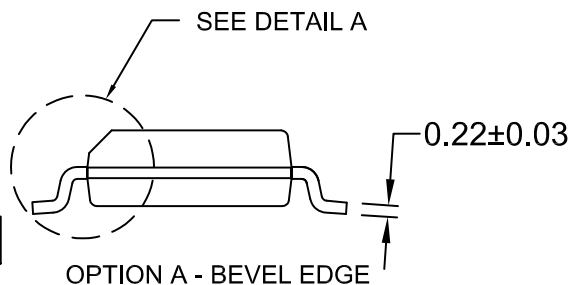
⌀ 0.25 (M) C B A



LAND PATTERN RECOMMENDATION



0.10



DETAIL A

SCALE: 2:1

NOTES:

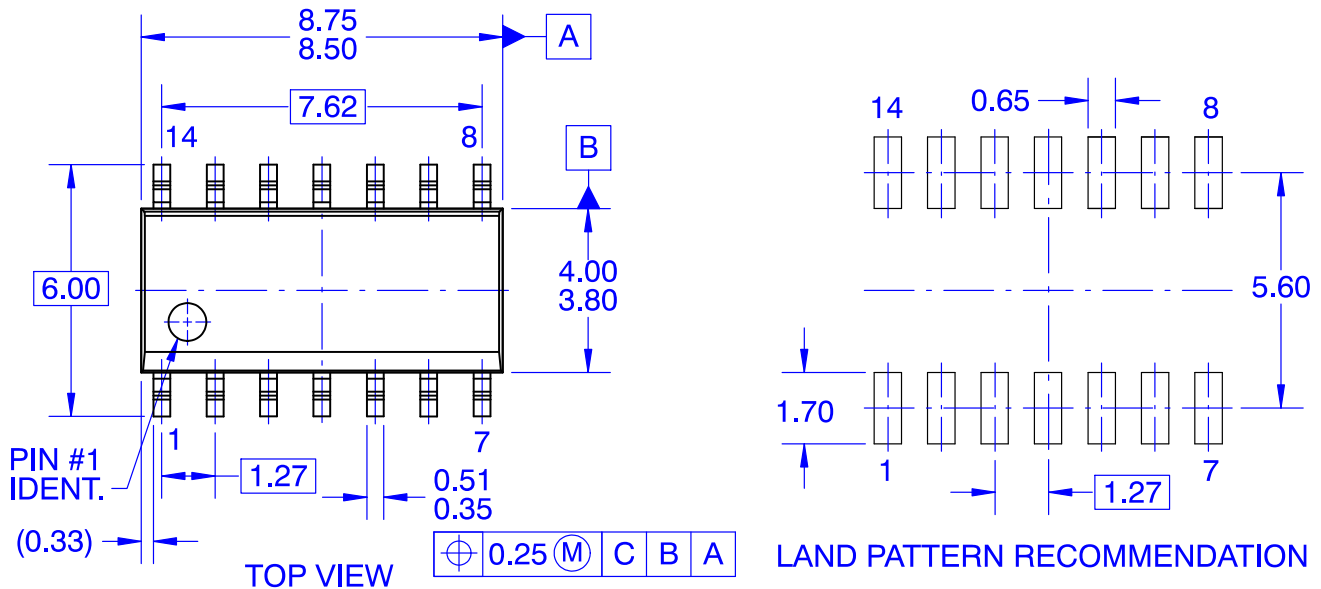
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

DOCUMENT NUMBER:	98AON13735G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC8	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

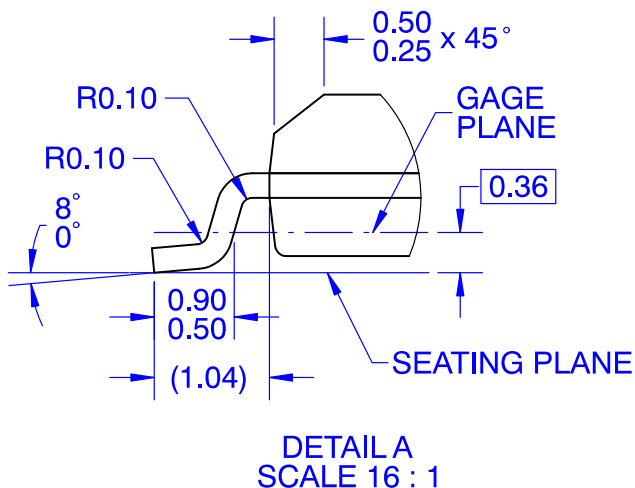
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



DOCUMENT NUMBER:	98AON13739G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC14	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales