Current Mode Resonant Controller, with Integrated High-Voltage Drivers, High Performance

NCP1399 Series

The NCP1399 is a high performance current mode controller for half bridge resonant converters. This controller implements 600 V gate drivers, simplifying layout and reducing external component count. The built−in Brown−Out input function eases implementation of the controller in all applications. In applications where a PFC front stage is needed, the NCP1399 features a dedicated output to drive the PFC controller. This feature together with dedicated skip mode technique further improves light load efficiency of the whole application. The NCP1399 provides a suite of protection features allowing safe operation in any application. This includes: overload protection, over−current protection to prevent hard switching cycles, brown−out detection, open optocoupler detection, automatic dead−time adjust, overvoltage (OVP) and overtemperature (OTP) protections.

Features

- High−Frequency Operation from 20 kHz up to 750 kHz
- Current Mode Control Scheme
- Automatic Dead−time with Maximum Dead−time Clamp
- Dedicated Startup Sequence for Fast Resonant Tank Stabilization
- Skip Mode Operation for Improved Light Load Efficiency
- Off−mode Operation for Extremely Low No−load Consumption
- Latched or Auto−Recovery Overload Protection
- Latched or Auto−Recovery Output Short Circuit Protection
- Latched Input for Severe Fault Conditions, e.g. OVP or OTP
- Out of Resonance Switching Protection
- Open Feedback Loop Protection
- Precise Brown−Out Protection
- PFC Stage Operation Control According to Load Conditions
- Startup Current Source with Extremely Low Leakage Current
- Dynamic Self−Supply (DSS) Operation in Off−mode or Fault Modes
- Pin to Adjacent Pin / Open Pin Fail Safe
- These are Pb−Free Devices

Typical Applications

- Adapters and Offline Battery Chargers
- Flat Panel Display Power Converters
- Computing Power Supplies
- Industrial and Medical Power Sources

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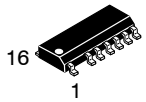
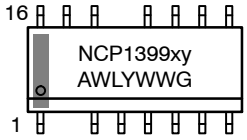


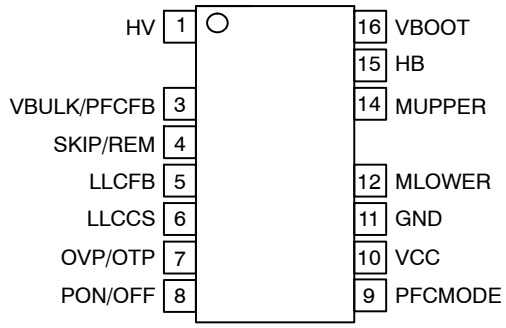
SOIC−16 NB
(LESS PINS 2 AND 13)
D SUFFIX
CASE 751DU

MARKING DIAGRAM



NCP1399 = Specific Device Code
xy = Specific Device Option
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

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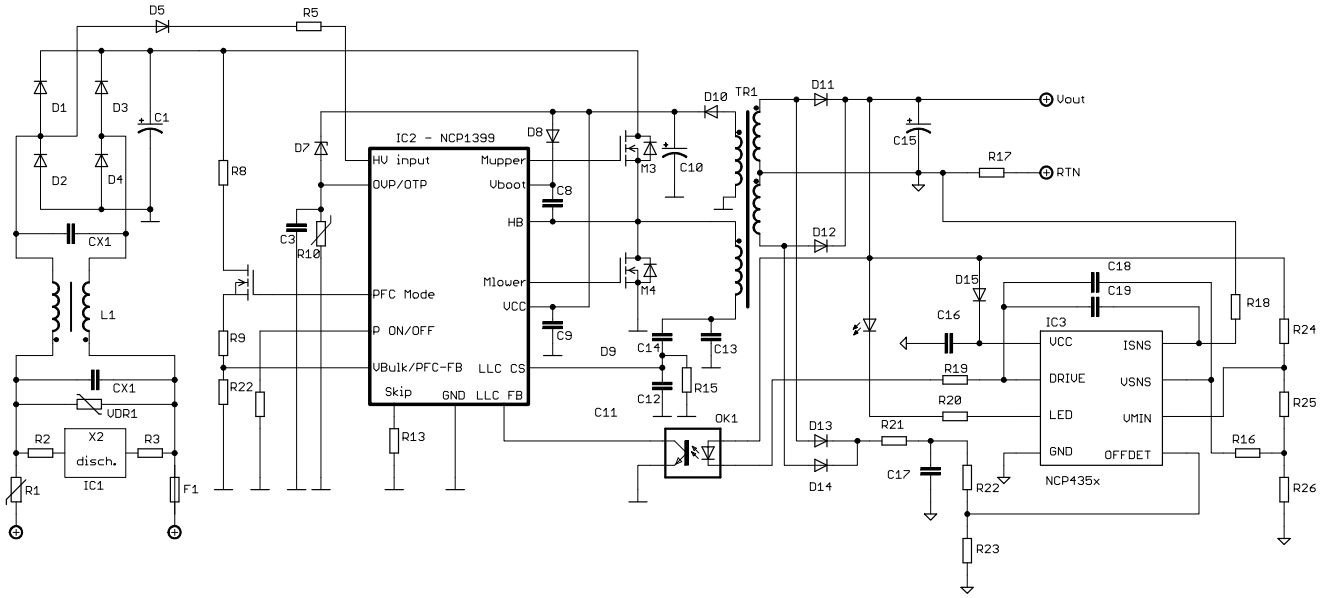


Figure 1. Typical Application Example without PFC Stage − WLLC Design (Active OFF off−mode)

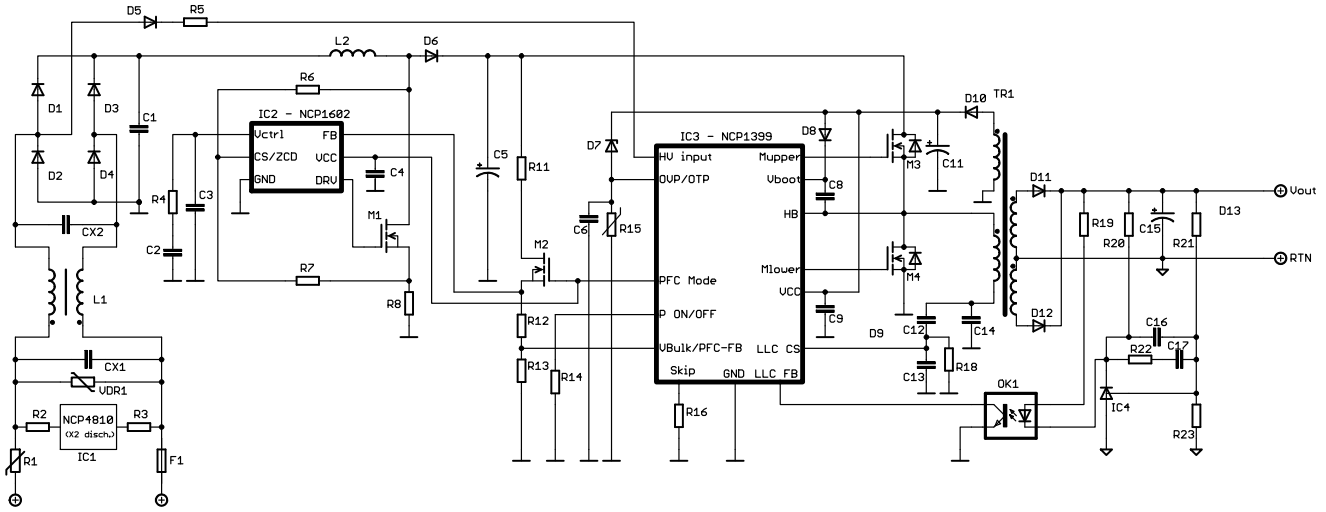


Figure 2. Typical Application Example with PFC Stage (Active OFF off−mode)

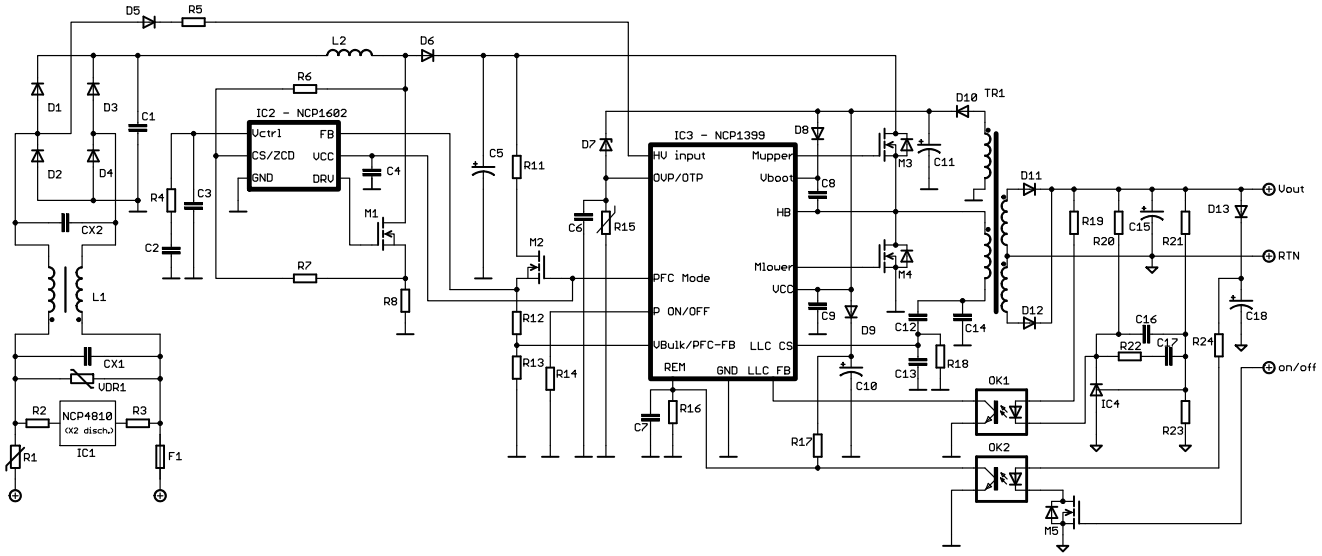


Figure 3. Typical Application Example with PFC Stage (Active ON off−mode)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	HV	High − voltage startup current source input	Connects to rectified AC line or to bulk capacitor to perform functions of Start − up Current Source and Dynamic Self − Supply
2	NC	Not connected	Increases the creepage distance
3	VBULK / PFC FB	Bulk voltage monitoring input	Receives divided bulk voltage to perform Brown−out protection.
4	SKIP/REM	Skip threshold adjust / Off−mode control input	Sets the skip in threshold via a resistor connected to ground − version NCP1399Ay. Activates off−mode (or Standby) when pulled−up by external auxiliary voltage source / deactivates off−mode when pull down by external off−mode control optocoupler − version NCP1399By.
5	LLC FB	LLC feedback input	Defines operating frequency based on given load conditions. Activates skip mode operation under light load conditions. Activates off−mode operation for NCP1399Ay version.
6	LLC CS	LLC current sense input	Senses divided resonant capacitor voltage to perform on−time modulation, out of resonant switching protection, over−current protection and secondary side short circuit protection.
7	OTP / OVP	Over−temperature and over−voltage protection input	Implements over−temperature and over−voltage protection on single pin.
8	P ON/OFF	PFC turn−off FB level adjust	Adjusts the FB pin to a level below which the PFC stage operation is disabled.
9	PFC MODE	PFC and external HV switch control output	Provides supply voltage for PFC front stage controller and/or enables Vbulk sensing network HV switch.
10	VCC	Supplies the controller	The controller accepts up to 20 V on VCC pin
11	GND	Analog ground	Common ground connection for adjust components, sensing networks and DRV outputs.
12	MLOWER	Low side driver output	Drives the lower side MOSFET
13	NC	Not connected	Increases the creepage distance
14	MUPPER	High side driver output	Drives the higher side MOSFET
15	HB	Half − bridge connection	Connects to the half − bridge output.
16	VBOOT	Bootstrap pin	The floating VCC supply for the upper stage

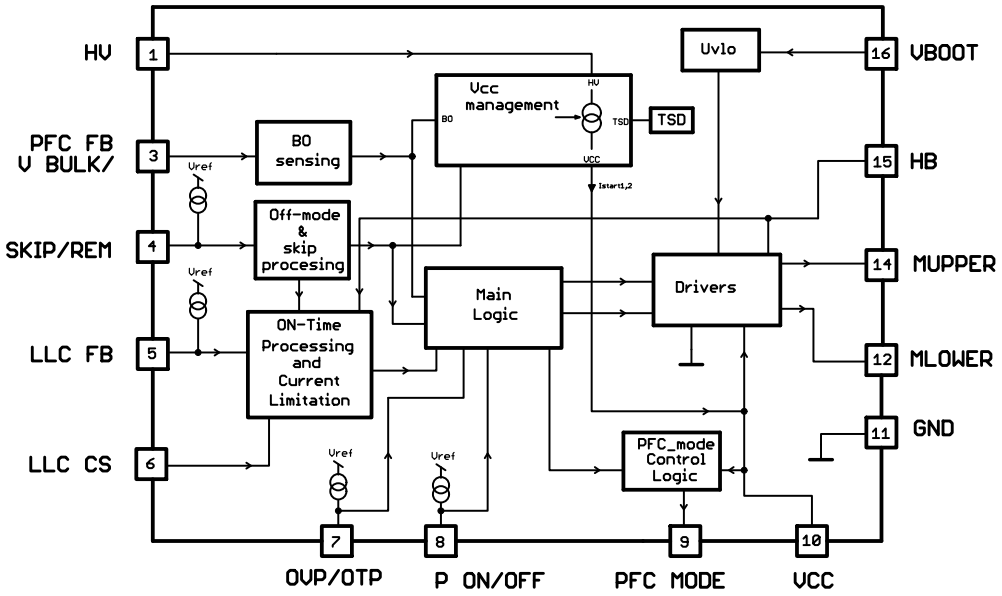


Figure 4. Internal Circuit Architecture

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
HV Startup Current Source HV Pin Voltage (Pin 1)		V_{HV}	−0.3 to 600	V
VBULK/PFC FB Pin Voltage (Pin3)		$V_{BULK/PFC\ FB}$	−0.3 to 5.5	V
SKIP/REM Pin Voltage (Pin 4) NCP1399Ay Revision Only		$V_{SKIP/REM}$	−0.3 to 5.5	V
SKIP/REM Pin Voltage (Pin 4) NCP1399By Revision Only		$V_{SKIP/REM}$	−0.3 to 10	V
LLC FB Pin Voltage (Pin 5)		V_{FB}	−0.3 to 5.5	V
LLC CS Pin Voltage (Pin 6)		V_{CS}	−5 to 5	V
PFC MODE Pin Output Voltage (Pin 9)		$V_{PFC\ MODE}$	−0.3 to V_{CC} + 0.3	V
VCC Pin Voltage (Pin 10)		V_{CC}	−0.3 to 20	V
Low Side Driver Output Voltage (Pin 12)		V_{DRV_MLOWER}	−0.3 to V_{CC} + 0.3	V
High Side Driver Output Voltage (Pin 14)		V_{DRV_MUPPER}	V_{HB} − 0.3 to V_{BOOT} + 0.3	V
High Side Offset Voltage (Pin 15)		V_{HB}	V_{Boot} −20 to V_{Boot} +0.3	V
High Side Floating Supply Voltage (Pin 16)	T_J = −40°C to +125°C T_J = −55°C to −40°C	V_{BOOT}	−0.3 to 620 −0.3 to 618	V
High Side Floating Supply Voltage (Pin 15 and 16)		$V_{Boot-VHB}$	−0.3 to 20.0	V
Allowable Output Slew Rate on HB Pin (Pin 15)		dV/dt_{max}	50	V/ns
OVP/OTP Pin Voltage (Pin 7)		$V_{OVP/OTP}$	−0.3 to 5.5	V
P ON/OFF Pin Voltage (Pin 8)		$V_{P\ ON/OFF}$	−0.3 to 5.5	V
Junction Temperature		T_J	−55 to 150	°C
Storage Temperature		T_{STG}	−55 to 150	°C
Thermal Resistance Junction−to−air		$R_{\theta JA}$	130	°C/W
Human Body Model ESD Capability per JEDEC JESD22−A114F (except HV Pin − Pin 1)		−	4.5	kV
Charged−Device Model ESD Capability per JEDEC JESD22−C101E		−	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
HV Startup Current Source						
V_{HV_MIN1}	Minimum voltage for current source operation (V_{CC} = V_{CC_ON} −0.5 V, I_{START2} drops to 95 %)	1	–	–	60	V
V_{HV_MIN2}	Minimum voltage for current source operation (V_{CC} = V_{CC_ON} −0.5 V, I_{START2} drops to 5 mA)	1	–	–	60	V
I_{START1}	Current flowing out of V_{CC} pin (V_{CC} = 0 V)	1, 10	0.2	0.5	0.8	mA
I_{START2}	Current flowing out of V_{CC} pin (V_{CC} = V_{CC_ON} −0.5 V)	1, 10	6	9	13	mA
I_{START_OFF}	Off−state leakage current (V_{HV} = 500 V, V_{CC} = 15 V)	1	–	–	10	μA
$I_{HV_OFF-MODE}$	HV pin current when off−mode operation is active (V_{HV} = 400 V)	1	–	–	8	μA
Supply Section						
V_{CC_ON}	Turn−on threshold level, V_{CC} going up	10	15.3	15.8	16.3	V
V_{CC_ON}	Turn−on threshold level, V_{CC} going up (NCP1399AL, NCP1399AM, NCP1399AR, NCP1399AS)	10	11.5	12.0	12.3	V
V_{CC_OFF}	Minimum operating voltage after turn−on	10	9.0	9.5	10	V
V_{CC_RESET}	V_{CC} level at which the internal logic gets reset	10	5.8	6.6	7.2	V
$V_{CC_INHIBIT}$	V_{CC} level for I_{START1} to I_{START2} transition	10	0.40	0.80	1.25	V
$V_{CC_ON_BLANK}$	Delay to generate DRVs pulses after V_{CC_ON} is reached	10	100	125	150	μs
$I_{CC_OFF-MODE}$	Controller supply current in off−mode, V_{CC} = V_{CC_ON} − 0.2 V (except NCP1399AG)	10, 11	10	27	40	μA
$I_{CC_SKIP-MODE}$	Controller supply current in skip−mode, V_{CC} = 15 V (NCP1399AA, BA, AC, AH, AI, AK, AM, AN, AP, AR, AS) (NCP1399AF, NCP1399AG, NCP1399AJ, NCP1399AT) (NCP1399AL)	10, 11	 580 500 500	 750 670 710	 900 820 890	μA
I_{CC_LATCH}	Controller supply current in latch−off mode, V_{CC} = V_{CC_ON} − 0.2 V (except NCP1399AI, AN, AP)	10, 11	330	490	600	μA
$I_{CC_AUTOREC}$	Controller supply current in auto−recovery mode, V_{CC} = V_{CC_ON} − 0.2 V (except NCP1399AF, AT)	10, 11	300	490	600	μA
$I_{CC_OPERATION}$	Controller supply current in normal operation, f_{sw} = 100 kHz, C_{load} = 1 nF, V_{CC} = 15 V	10, 11	4.0	5.4	7.0	mA
Bootstrap Section						
V_{BOOT_ON}	Startup voltage on the floating section (Note 5)	16, 15	8	9	10	V
V_{BOOT_OFF}	Cutoff voltage on the floating section	16, 15	7.2	8.2	9.0	V
I_{BOOT1}	Upper driver consumption, no DRV pulses	16, 15	30	75	130	μA
I_{BOOT2}	Upper driver consumption, C_{load} = 1 nF between Pins 13 & 15 f_{sw} = 100 kHz, HB connected to GND	16, 15	1.30	1.65	2.00	mA
HB Discharger						
$I_{DISCHARGE1}$	HB sink current capability V_{HB} = 30 V	15	5	–	–	mA
$I_{DISCHARGE2}$	HB sink current capability V_{HB} = V_{HB_MIN}	15	1	–	–	mA
V_{HB_MIN}	HB voltage @ $I_{DISCHARGE}$ changes from 2 to 0 mA	15	–	–	10	V
Remote Input – NCP1399By						
V_{REM_ON}	Remote pin voltage below which off−mode is deactivated (V_{REM} going down)	4	1.0	1.5	2.0	V
V_{REM_OFF}	Remote pin voltage above which off−mode is activated (V_{REM} going up)	4	7.2	8.0	8.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The NCP1399Ay version has skip adjustable externally.
3. Guaranteed by design.
4. Minimal impedance on P ON/OFF pin is 1 kΩ
5. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Remote Input – NCP1399By						
t_{REM_TIMER}	Remote timer duration	4	80	100	120	ms
I_{REM_LEAK}	Remote input leakage current (V_{REM} = 10 V)	4	–	0.02	1.00	μA
R_{SW_REM}	Internal remote pull down switch resistance (V_{REM} = 8 V)	4	3	–	7	kΩ
Remote Control – NCP1399Ay (i.e. Off−mode is Sensed via FB Pin, except NCP1399AG)						
$V_{FB_REM_ON}$	FB pin voltage above which off−mode is deactivated (V_{FB} going up)	5	1.5	2.0	2.5	V
$V_{FB_REM_OFF}$	FB pin voltage below which off−mode is activated (V_{FB} going down)	5	0.36	0.40	0.44	V
$I_{FB_REM_BIAS}$	Pull−up FB pin bias current during off−mode	5	1.0	2.3	4.0	μA
Driver Outputs						
t_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	12, 14	20	45	80	ns
t_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	12, 14	5	30	50	ns
R_{OH}	Source resistance	12, 14	4	16	32	Ω
R_{OL}	Sink resistance	12, 14	1	5	11	Ω
$I_{DRVSOURCE}$	Output high short circuit pulsed current V_{DRV} = 0 V, PW ≤ 10 μs	12, 14	–	0.5	–	A
$I_{DRVSINK}$	Output high short circuit pulsed current V_{DRV} = VCC, PW ≤ 10 μs	12, 14	–	1	–	A
I_{HV_LEAK}	Leakage current on high voltage pins to GND	14, 15, 16	–	–	5	μA
Dead−time Generation						
$t_{DEAD_TIME_MAX}$	Maximum Dead−time value if no dV/dt falling/rising edge is received	12, 14	720	800	880	ns
N_{DT_MAX}	Number of DT_MAX events to enters IC into fault (NCP1399AA, BA, AH, AK, AL, AR)	12, 14, 16	–	8	–	–
	Number of DT_MAX events to enters IC into fault (NCP1399AC, AF, AG, AI, AJ, AM, AN, AP, AS, AT)	12, 14, 16	–	16	–	–
dV/dt Detector						
P_{dV/dt_th}	Positive slew rate on V_{BOOT} pin above which automatic dead−time end is generated	16	–	210	–	V/μs
N_{dV/dt_th}	Negative slew rate on V_{BOOT} pin above which automatic dead−time end is generated	16	–	210	–	V/μs
PFC MODE Output and P ON/OFF Adjust						
$V_{PFC_M_BO}$	PFC MODE output voltage when V_{FB} < $V_{P\ ON/OFF}$ (sink 1 mA current from PFC MODE output)	9	5.75	6.00	6.25	V
$V_{PFC_M_ON}$	PFC MODE output voltage when V_{FB} > $V_{P\ ON/OFF}$ (sink 10 mA current from PFC MODE output)	9	V_{CC} − 0.4	–	–	V
$I_{PFC_M_LIM}$	PFC MODE output current limit ($V_{PFC\ MODE}$ < 2 V)	9	0.7	1.2	1.85	mA
$t_{P\ ON/OFF_TIMER}$	Delay to transition PFC MODE from $V_{PFC_M_ON}$ to $V_{PFC_M_BO}$ after V_{FB} drops below $V_{P\ ON/OFF}$	5, 8, 9	9.4	–	10.9	s
$I_{P\ ON/OFF}$	Pull−up current source (Note 4)	8	18	20	22	μA
P ON/OFF_{HYST}	P ON/OFF comparator hysteresis – percentage level of P ON/OFF pin voltage	5, 8, 9	80	100	120	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The NCP1399Ay version has skip adjustable externally.
3. Guaranteed by design.
4. Minimal impedance on P ON/OFF pin is 1 kΩ
5. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
OVP/OTP						
V_{OVP}	OVP threshold voltage ($V_{OVP/OTP}$ going up)	7	2.35	2.50	2.65	V
V_{OTP}	OTP threshold voltage ($V_{OVP/OTP}$ going down)	7	0.76	0.80	0.84	V
I_{OTP}	OTP/OVP pin source current for external NTC − during normal operation	7	90	95	100	μA
I_{OTP_BOOST}	OTP/OVP pin source current for external NTC − during startup	7	180	190	200	μA
t_{OVP_FILTER}	Internal filter for OVP comparator	7	32	37	44	μs
t_{OTP_FILTER}	Internal filter for OTP comparator	7	200	330	500	μs
t_{BLANK_OTP}	Blanking time for OTP input during startup (NCP1399AA, NCP1399BA, NCP1399AK, NCP1399AR)	7	7.3	8.0	8.7	ms
	Blanking time for OTP input during startup (NCP1399AC, AF, AG, AH, AI, AJ, AL, AM, AN, AP, AS, AT)	7	14	16	18	ms
V_{CLAMP_OVP/OTP_1}	OVP/OTP pin clamping voltage @ $I_{OVP/OTP}$ = 0 mA	7	1.0	1.2	1.4	V
V_{CLAMP_OVP/OTP_2}	OVP/OTP pin clamping voltage @ $I_{OVP/OTP}$ = 1 mA	7	1.8	2.4	3.0	V
Start−up Sequence Parameters						
t_{TON_MAX}	Maximum on−time clamp (NCP1399AA, BA, AK, AL, AR)	12, 14	7.3	7.7	8.4	μs
	Maximum on−time clamp (NCP1399AC, AG, AI, AM, AN, AP)	12, 14	10.6	11.2	12.1	μs
	Maximum on−time clamp (NCP1399AF, AJ, AS, AT)	12, 14	15.2	16.3	17.8	μs
	Maximum on−time clamp (NCP1399AH)	12, 14	8.8	9.5	10.5	μs
$t_{1st_MLOWER_TON}$	Initial Mlower DRV on−time duration (NCP1399AA, BA, AC, AG, AH, AI, AK, AL, AM, AN, AP, AR, AS, AT)	12	4.7	4.9	5.4	μs
$t_{1st_MLOWER_TON}$	Initial Mlower DRV on−time duration (NCP1399AF, NCP1399AJ)	12	9.3	10	11	μs
$t_{1st_MUPPER_TON}$	Initial Mupper DRV on−time duration (NCP1399AM)	14	0.44	0.50	0.57	μs
$t_{1st_MUPPER_TON}$	Initial Mupper DRV on−time duration (NCP1399AR)	14	0.15	0.20	0.25	μs
$t_{1st_MUPPER_TON}$	Initial Mupper DRV on−time duration (NCP1399AA, BA, AC, AG, AH, AI, AK, AL, AN, AP, AT) (NCP1399AS)	14	 0.72 2.07	 0.79 2.30	 0.88 2.53	μs
$t_{1st_MUPPER_TON}$	Initial Mupper DRV on−time duration (NCP1399AF, NCP1399AJ)	14	0.99	1.10	1.21	μs
$t_{SS_INCREMENT}$	On−time period increment during soft−start (NCP1399AA, BA, AC, AG, AH, AI, AK, AL, AM, AN, AP, AR, AT) (NCP1399AS)	12, 14	 17 37	 20 40	 22 44	ns
$t_{SS_INCREMENT}$	On−time period increment during soft−start (NCP1399AF, NCP1399AJ)	12, 14	75	80	88	ns
$K_{SS_INCREMENT}$	Soft−Start increment division ratio (NCP1399AA, BA, AK, AS)	12, 14	−	4	−	−
	Soft−Start increment division ratio (NCP1399AL)	12, 14	−	2	−	−
	Soft−Start increment division ratio (NCP1399AC, AF, AG, AH, AI, AJ, AM, AN, AP, AR, AT)	12, 14	−	8	−	−
$t_{WATCHDOG}$	Time duration to restart IC if start−up phase is not finished	12, 14	0.45	0.50	0.55	ms
Feedback Section						
R_{FB}	Internal pull−up resistor on FB pin	5	15	18	25	kΩ
K_{FB}	V_{FB} to internal current set point division ratio	5	1.92	2.00	2.08	−
V_{FB_REF}	Internal voltage reference on the FB pin	5	4.60	4.95	5.30	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The NCP1399Ay version has skip adjustable externally.
3. Guaranteed by design.
4. Minimal impedance on P ON/OFF pin is 1 kΩ
5. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Feedback Section						
V_{FB_CLAMP}	Internal clamp on FB input of On−time comparator referred to external FB pin voltage	5	4.4	4.6	4.8	V
$V_{FB_SKIP_IN}$	Feedback voltage thresholds to enters in skip mode for NCP1399By version (Note 2)	5	0.44	0.50	0.56	V
$V_{FB_SKIP_HYST}$	Skip comparator hysteresis (NCP1399AR)	5	638	730	862	mV
	Skip comparator hysteresis (NCP1399AA, BA, AC, AG, AH, AK, AM, AP, AS)	5	130	160	200	mV
	Skip comparator hysteresis (NCP1399AF, AJ, AL, AT)	5	105	140	175	mV
	Skip comparator hysteresis (NCP1399AI, NCP1399AN)	5	0	23	50	mV
$t_{1st_MLOWER_SKIP}$	On−time duration of 1st Mlower pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AA, NCP1399BA, NCP1399AK, NCP1399AL)	5, 12	0.95	1.05	1.15	μs
	On−time duration of 1st Mlower pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AC, AG, AI, AM, AN, AP, AS)	5, 12	1.8	1.9	2.1	μs
	On−time duration of 1st Mlower pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AF, NCP1399AJ, NCP1399AT)	5, 12	1.08	1.20	1.32	μs
	On−time duration of 1st Mlower pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AR)	5, 12	1.89	2.05	2.31	μs
	On−time duration of 1st Mlower pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AH)	5, 12	2.1	2.4	2.7	μs
$V_{1st_MUPPER_SKIP}$	Internal FB level reduction during 1st Mupper pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AR) (Note 3)	5, 6, 14	–	500	–	mV
	Internal FB level reduction during 1st Mupper pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AA, BA, AC, AG, AI, AK, AL, AM, AN, AP, AS) (Note 3)	5, 6, 14	–	150	–	mV
	Internal FB level reduction during 1st Mupper pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AF, NCP1399AJ, NCP1399AT) (Note 3)	5, 6, 14	–	100	–	mV
	Internal FB level reduction during 1st Mupper pulse when FB cross $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold (NCP1399AH) (Note 3)	5, 6, 14	–	0	–	mV
Skip Input – NCP1399Ay version						
I_{SKIP}	Internal Skip pin current source	4	48	50	52	μA
$C_{SKIP_LOAD_MAX}$	Maximum loading capacitance for skip pin voltage filtering (Note 3)	4	–	–	10	nF
Current Sense Input Section						
t_{pd_CS}	On−time comparator delay to Mupper driver turn off V_{FB} = 2.5 V, V_{CS} goes up from −2.5 V to 2.5 V with rising edge of 100 ns	5, 6	–	–	250	ns
$I_{CS_LEAKAGE}$	Current sense input leakage current for V_{CS} = ±3 V	6	–	–	±1	μA
V_{CS_OFFSET}	Current sense input offset voltage (NCP1399AA, A, AC, AG, AH, AI, AK, AL, AM, AN, AP, AR, AS)	6	160	200	240	mV
	Current sense input offset voltage (NCP1399AF, AJ, AT)	6	110	150	190	mV
t_{LEB}	Leading edge blanking time of the on−time comparator output	5, 6, 14	360	440	540	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The NCP1399Ay version has skip adjustable externally.
3. Guaranteed by design.
4. Minimal impedance on P ON/OFF pin is 1 kΩ
5. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.)

Symbol	Rating	Pin	Min	Typ	Max	Unit
Faults and Auto−Recovery Timer						
$t_{FB_FAULT_TIMER}$	FB fault timer duration (NCP1399AA, BA, AK, AL, AR)	−	160	200	240	ms
	FB fault timer duration (NCP1399AC, AF, AG, AI, AJ, AM, AN, AP, AS, AT)	−	80	100	120	ms
	FB fault timer duration (NCP1399AH)	−	240	300	360	ms
$N_{FB_FAULT_COUNTER}$	Number of DRV pulses to confirm FB fault	−	−	1000	−	−
V_{FB_FAULT}	FB voltage when FB fault is detected	5	4.5	4.7	4.9	V
$N_{CS_FAULT_COUNTER}$	Number of CS_fault cmp. pulses to confirm CS fault	−	−	5	−	−
V_{CS_FAULT}	CS voltage when CS fault is detected (NCP1399AA, BA, AC, AF, AH, AI, AK, AL, AM, AN, AP, AR, AS, AT) (NCP1399AG) (NCP1399AJ)	6	 2.5 3.2 1.85	 2.7 3.4 2.00	 2.9 3.6 2.15	V
t_{A-REC_TIMER}	Auto−recovery duration, common timer for all fault condition (NCP1399AA, BA, AC, AG, AH, AJ, AK, AL, AM, AP, AR, AS)	−	0.8	1	1.2	s
	Auto−recovery duration, common timer for all fault condition (NCP1399AI, NCP1399AN)	−	1.6	1.9	2.4	
Brown−Out Protection						
V_{BO}	Brown−out turn−off threshold	3	0.965	1.000	1.035	V
I_{BO}	Brown−out hysteresis current, $V_{VBULK/PFC_FB} < V_{BO}$	3	4.3	5.0	5.4	μA
V_{BO_HYST}	Brown − Out comparator hysteresis	3	5	12	25	mV
I_{BO_BIAS}	Brown − Out input bias current	3	−	−	0.05	μA
t_{BO_FILTR}	BO filter duration	3	10	20	30	μs
Ramp Compensation						
RC_{GAIN}	Ramp compensation gain (NCP1399AA, BA, AC, AF AG, AK, AM, AP, AR, AT) Ramp compensation gain (NCP1399AI, NCP1399AN) Ramp compensation gain (NCP1399AJ) Ramp compensation gain (NCP1399AH) Ramp compensation gain (NCP1399AL) Ramp compensation gain (NCP1399AS)	−	 58 82 92 107 116 34	 82 110 125 149 166 47	 108 131 150 168 185 58	mV/μs
t_{RC_SHIFT}	Ramp compensation time shift	−	−	0.6	−	μs
Temperature Shutdown Protection						
T_{TSD}	Temperature shutdown T_J going up (NCP1399AA, BA, AH, AK, AR)	−	−	124	−	°C
	Temperature shutdown T_J going up (NCP1399AC, AF, AG, AI, AJ, AL, AM, AN, AP, AS, AT)	−	−	137	−	°C
T_{TSD_HYST}	Temperature shutdown hysteresis	−	−	30	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The NCP1399Ay version has skip adjustable externally.
3. Guaranteed by design.
4. Minimal impedance on P ON/OFF pin is 1 kΩ
5. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

IC Options

Option	FB fault	FB fault source	Cumulative FB fault timer/ counter	CS_FAULT	TON_MAX fault	OVP fault	OTP fault	Dedicated Soft_start_-seq
NCP1399AA	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399BA	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399AC	Auto−recovery	Timer	NO	Auto−recovery	OFF	Latch	Latch	ON
NCP1399AF	Latch	Timer	NO	Latch	Latch	Latch	Latch	ON
NCP1399AG	Auto−recovery	Timer	NO	Auto−recovery	OFF	Latch	Auto−recovery	ON
NCP1399AH	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399AI	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Auto−recovery	Auto−recovery	ON
NCP1399AJ	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Latch	ON
NCP1399AK	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399AL	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399AM	Auto−recovery	Timer	NO	Auto−recovery	OFF	Latch	Latch	ON
NCP1399AN	Auto−recovery	Timer	NO	Auto−recovery	OFF	Auto−recovery	Auto−recovery	ON
NCP1399AP	Auto−recovery	Timer	NO	Auto−recovery	OFF	Auto−recovery	Auto−recovery	ON
NCP1399AR	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON
NCP1399AS	Auto−recovery	Timer	NO	Auto−recovery	OFF	Latch	Latch	ON
NCP1399AT	Latch	Timer	NO	Latch	Latch	Latch	Latch	ON

Option	PFC_MODE skip status	Dead time control	Dead time fault	OFF−mode version	OFF−mode status	BO status	Ramp comp status	P ON/OFF pull−up
NCP1399AA	ON	ZVS or DT_max	Auto−recovery	Active OFF	ON	ON	Without ramp shift	ON
NCP1399BA	ON		Auto−recovery	Active ON	ON	ON		ON
NCP1399AC	ON		Auto−recovery	Active OFF	ON	ON		ON
NCP1399AF	OFF		OFF	Active OFF	ON	ON		ON
NCP1399AG	OFF		Auto−recovery	–	OFF	ON		ON
NCP1399AH	ON		OFF	Active OFF	ON	ON		ON
NCP1399AI	ON		Auto−recovery	Active OFF	ON	ON		ON
NCP1399AJ	OFF		OFF	Active OFF	ON	ON		ON
NCP1399AK	OFF		Auto−recovery	Active OFF	ON	ON		ON
NCP1399AL	ON		OFF	Active OFF	ON	ON		ON
NCP1399AM	ON		OFF	Active OFF	ON	ON		ON
NCP1399AN	ON		OFF	Active OFF	ON	ON		ON
NCP1399AP	ON		OFF	Active OFF	ON	ON		ON
NCP1399AR	ON		Auto−recovery	Active OFF	ON	ON		ON
NCP1399AS	ON		OFF	Active OFF	ON	ON		ON
NCP1399AT	OFF		OFF	Active OFF	ON	ON		ON

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
NCP1399AADR2G	NCP1399AA	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NCP1399BADR2G	NCP1399BA		
NCP1399ACDR2G	NCP1399AC		
NCP1399AFDR2G	NCP1399AF		
NCP1399AGDR2G	NCP1399AG		
NCP1399AHDR2G	NCP1399AH		
NCP1399AIDR2G	NCP1399AI		
NCP1399AJDR2G*	NCP1399AJ		
NCP1399AKDR2G	NCP1399AK		
NCP1399ALDR2G*	NCP1399AL		
NCP1399AMDR2G	NCP1399AM		
NCP1399ANDR2G	NCP1399AN		
NCP1399APDR2G	NCP1399AP		
NCP1399ARDR2G	NCP1399AR		
NCP1399ASDR2G	NCP1399AS		
NCP1399ATDR2G	NCP1399AT		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Available upon request.

TYPICAL CHARACTERISTICS

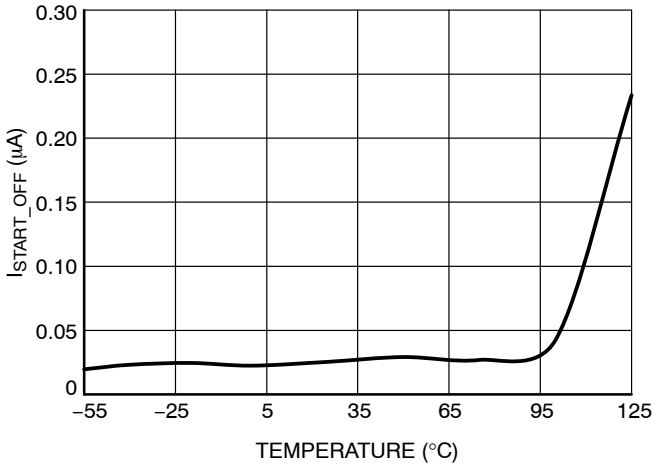


Figure 5. I_{START_OFF} vs. Temperature

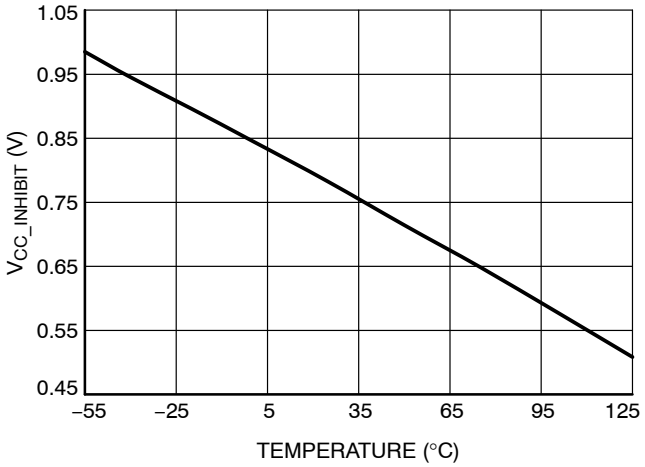


Figure 6. $V_{CC_INHIBIT}$ vs. Temperature

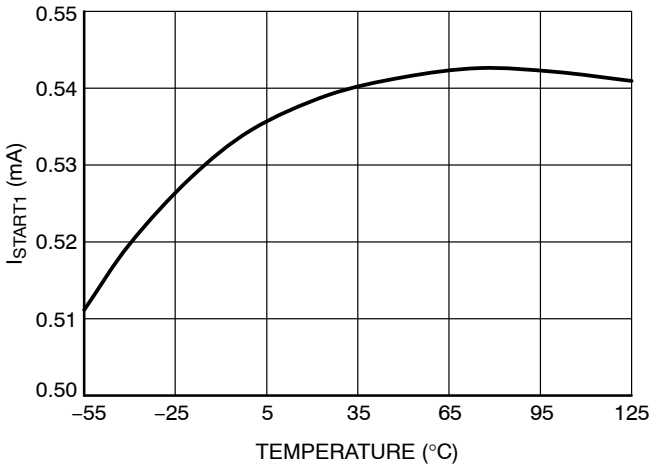


Figure 7. I_{START1} vs. Temperature

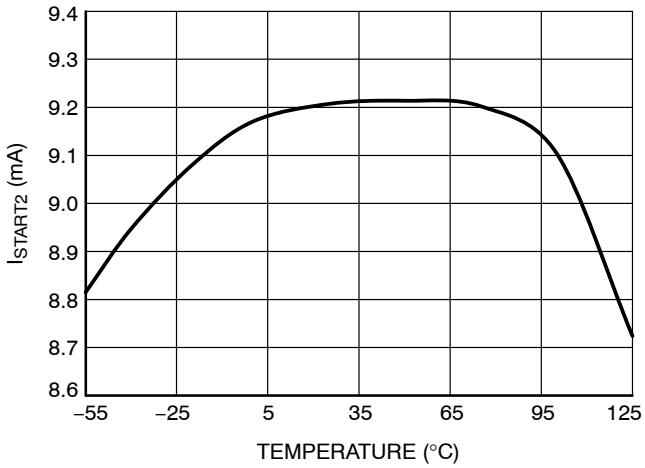


Figure 8. I_{START2} vs. Temperature

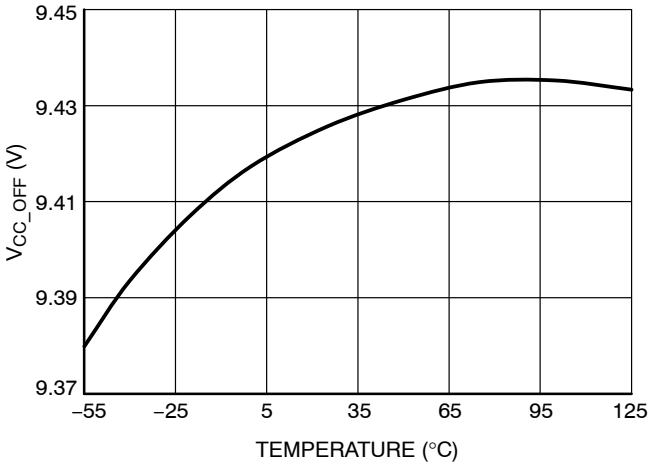


Figure 9. V_{CC_OFF} vs. Temperature

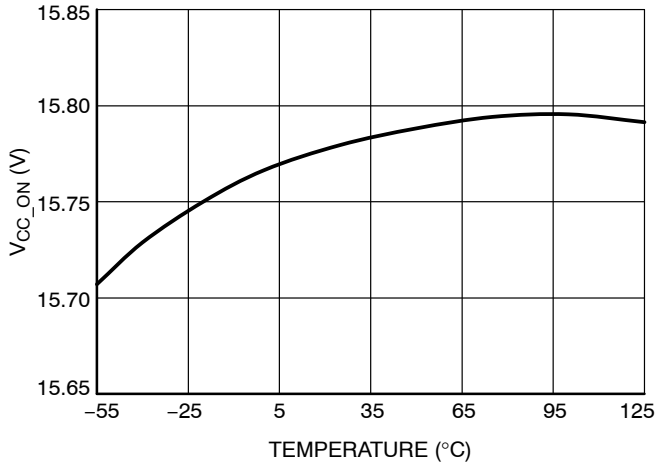


Figure 10. V_{CC_ON} vs. Temperature

TYPICAL CHARACTERISTICS

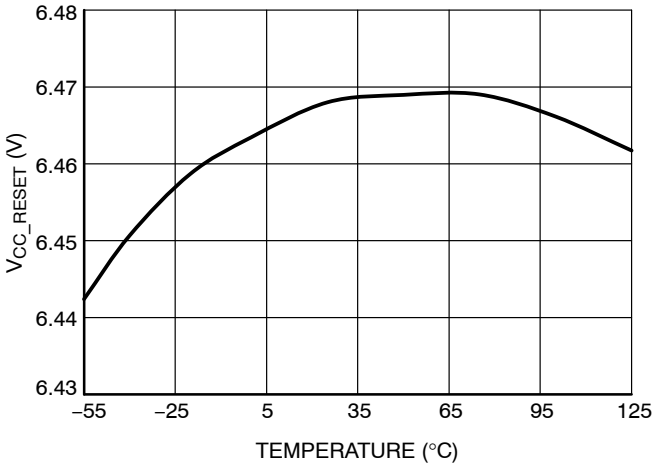


Figure 11. V_{CC_RESET} vs. Temperature

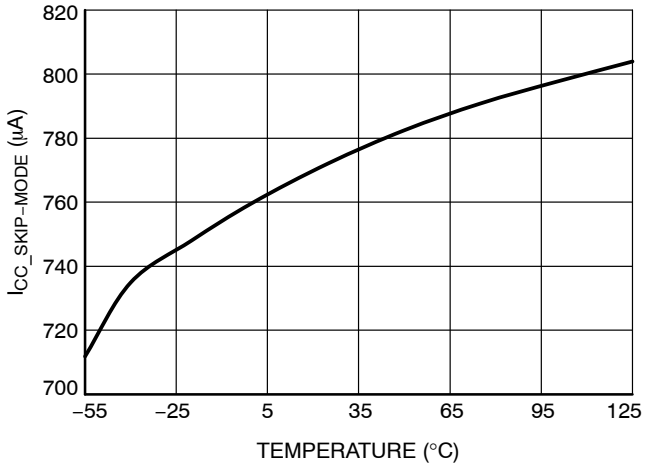


Figure 12. $I_{CC_SKIP−MODE}$ vs. Temperature

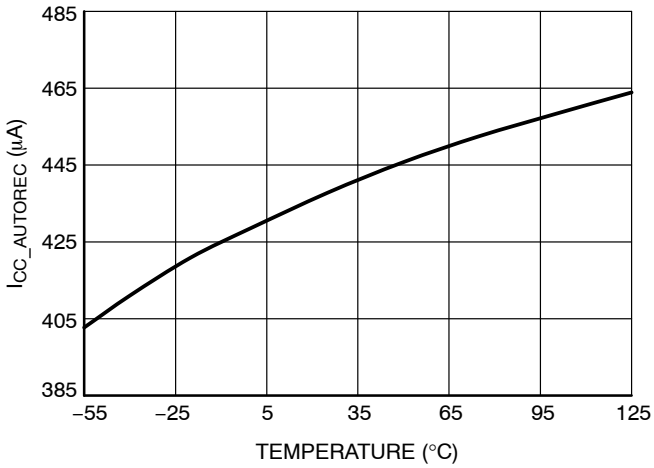


Figure 13. $I_{CC_AUTOREC}$ vs. Temperature

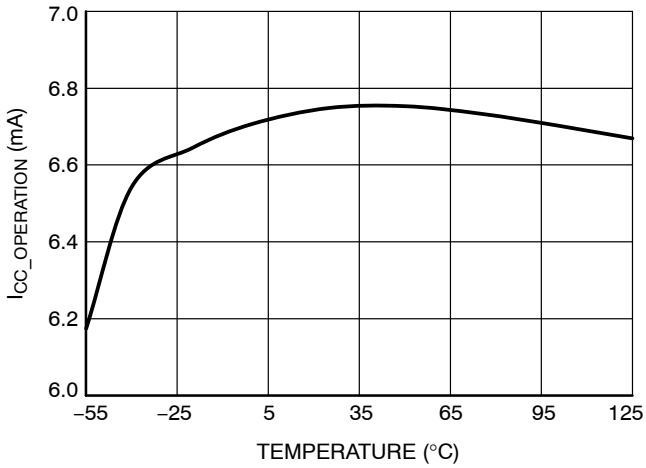


Figure 14. $I_{CC_OPERATION}$ vs. Temperature

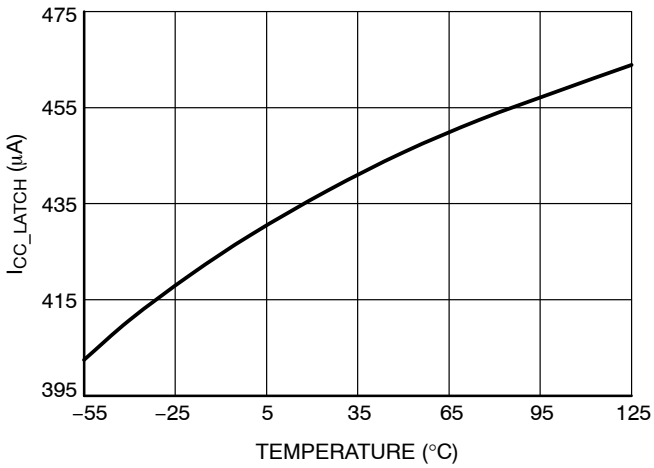


Figure 15. I_{CC_LATCH} vs. Temperature

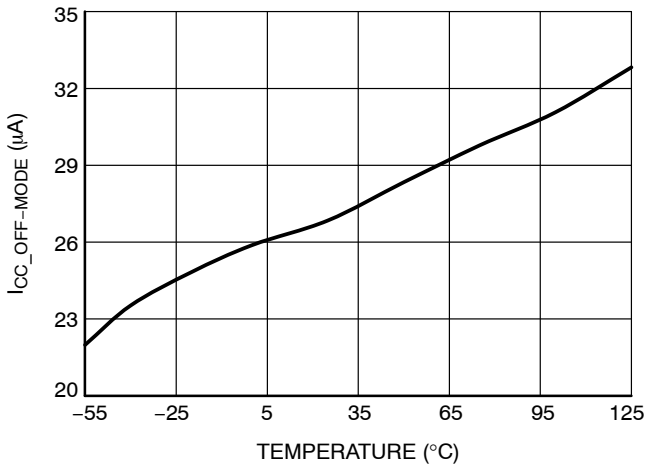


Figure 16. $I_{CC_OFF−MODE}$ vs. Temperature

TYPICAL CHARACTERISTICS

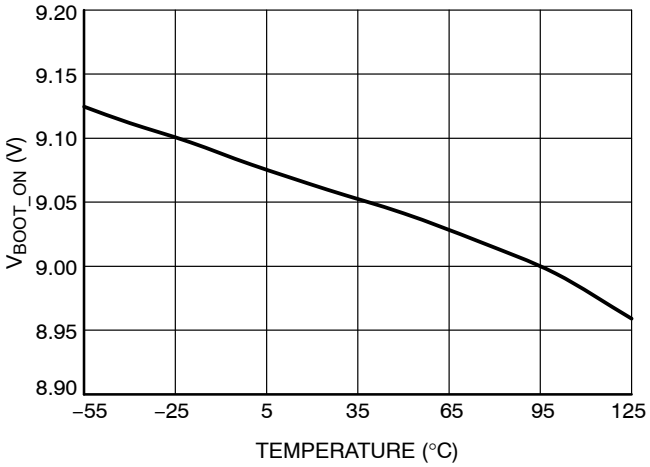


Figure 17. V_{BOOT_ON} vs. Temperature

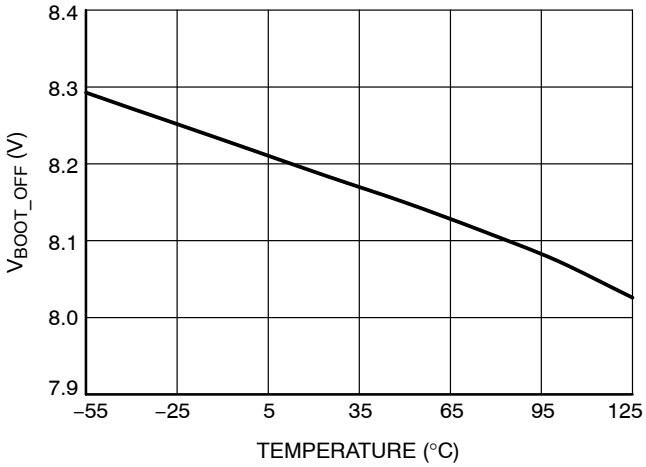


Figure 18. V_{BOOT_OFF} vs. Temperature

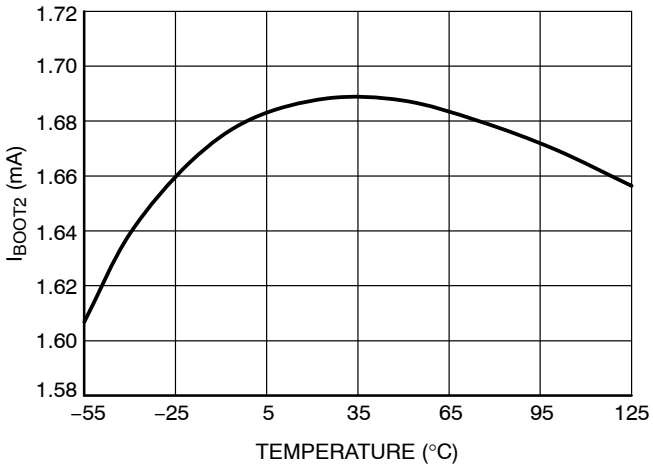


Figure 19. I_{BOOT2} vs. Temperature

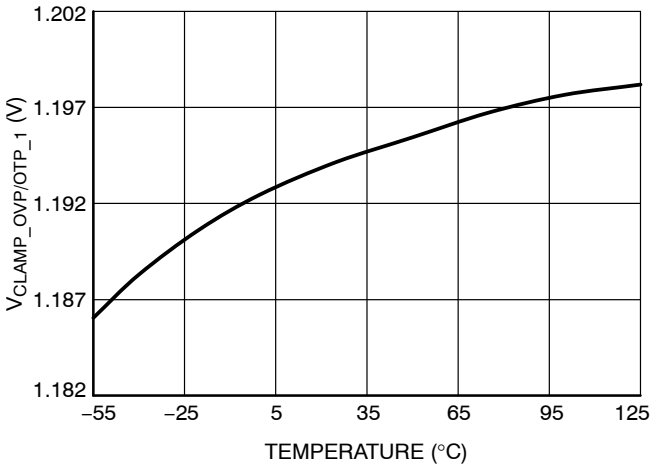


Figure 20. V_{CLAMP_OVP/OTP_1} vs. Temperature

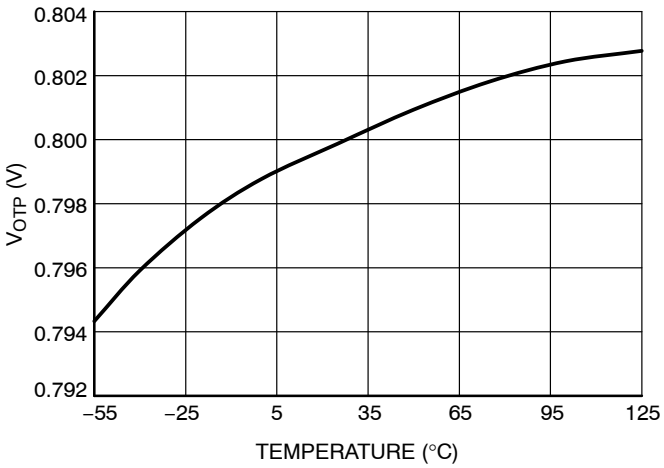


Figure 21. V_{OTP} vs. Temperature

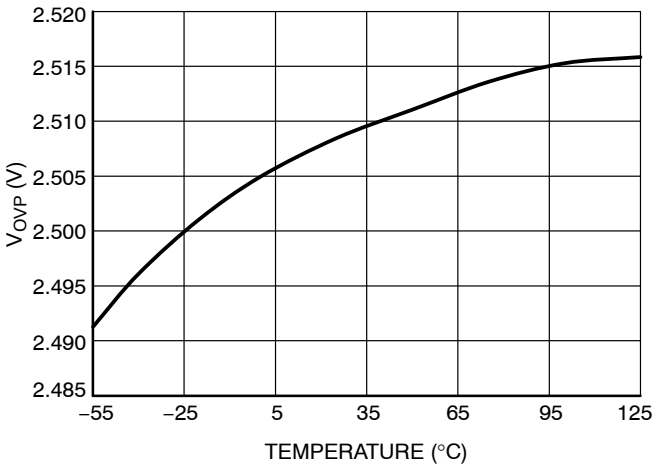


Figure 22. V_{OVP} vs. Temperature

TYPICAL CHARACTERISTICS

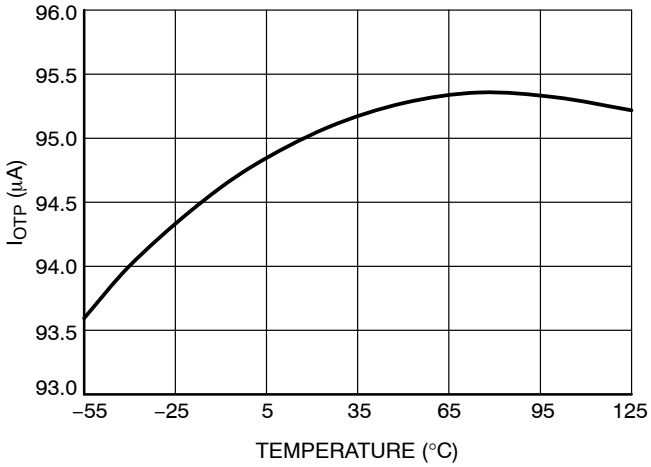


Figure 23. I_{OTP} vs. Temperature

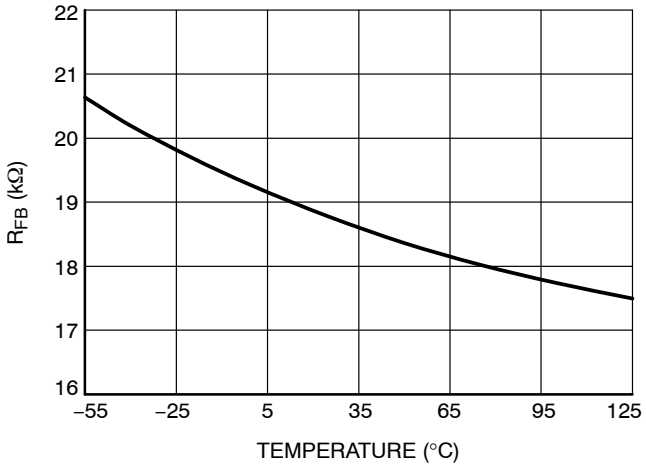


Figure 24. R_{FB} vs. Temperature

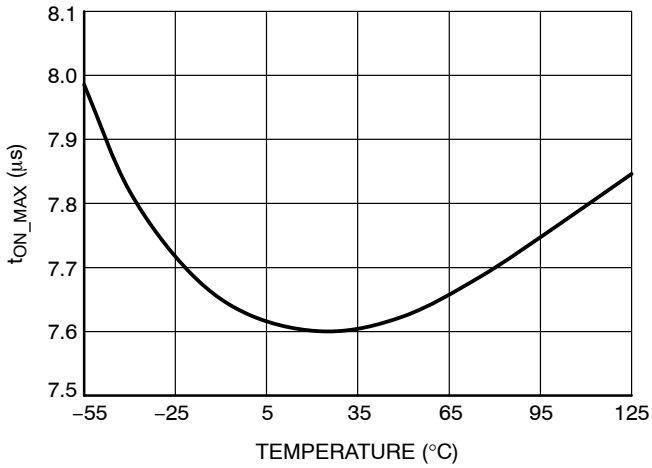


Figure 25. t_{ON_MAX} vs. Temperature

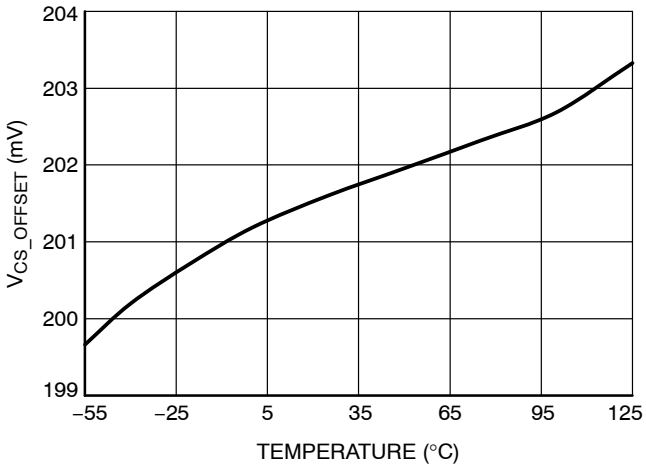


Figure 26. V_{CS_OFFSET} vs. Temperature

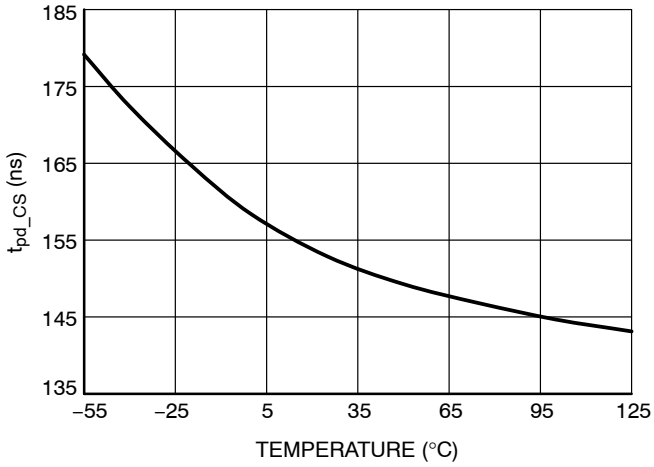


Figure 27. t_{pd_CS} vs. Temperature

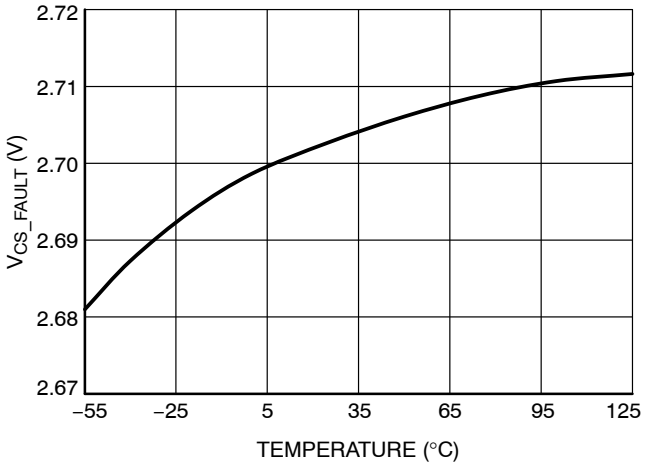


Figure 28. V_{CS_FAULT} vs. Temperature

TYPICAL CHARACTERISTICS

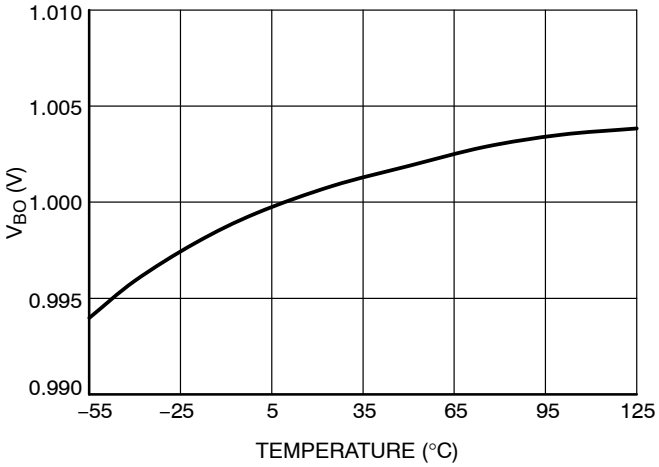


Figure 29. V_{BO} vs. Temperature

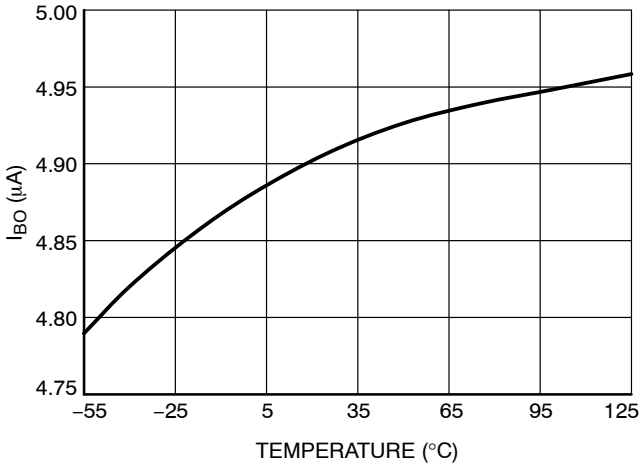


Figure 30. I_{BO} vs. Temperature

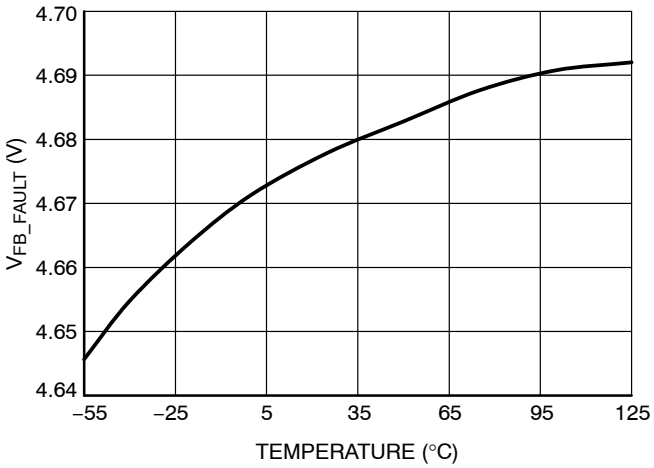


Figure 31. V_{FB_FAULT} vs. Temperature

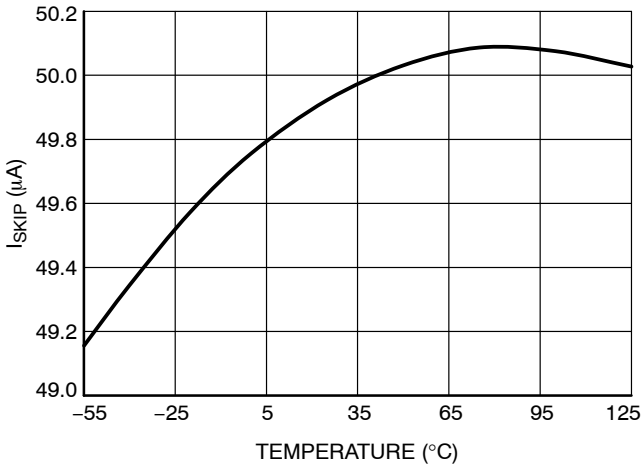


Figure 32. I_{SKIP} vs. Temperature

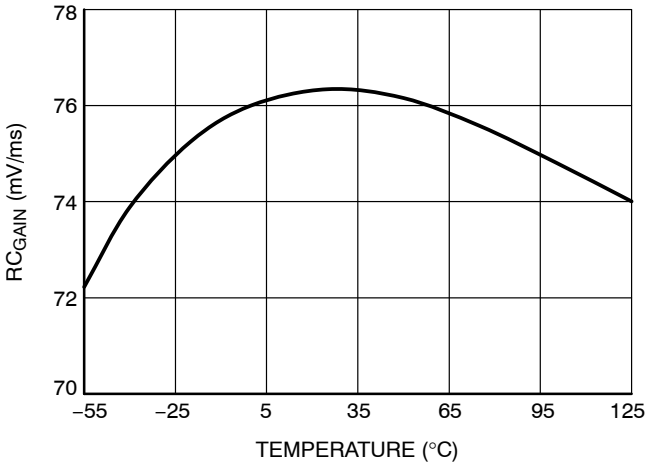


Figure 33. RC_{GAIN} vs. Temperature

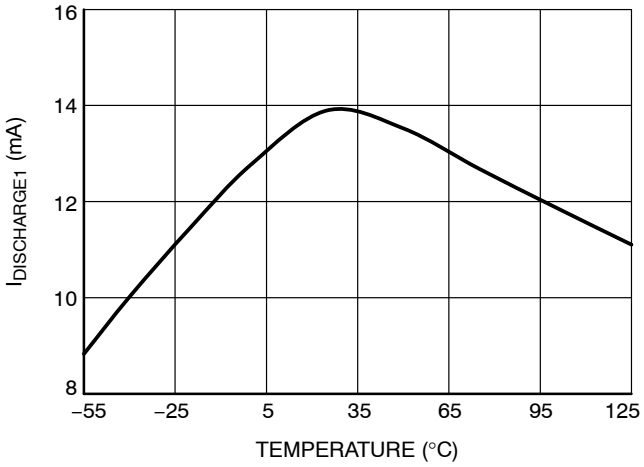


Figure 34. $I_{DISCHARGE1}$ vs. Temperature

TYPICAL CHARACTERISTICS

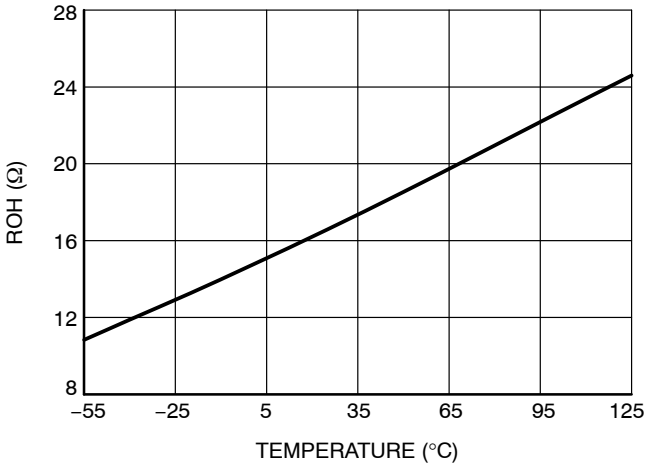


Figure 35. ROH vs. Temperature

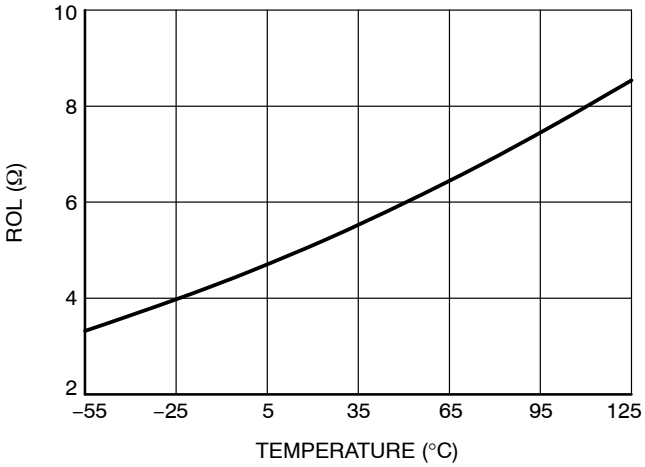


Figure 36. ROL vs. Temperature

VCC Management with High−voltage Startup Current Source

The NCP1399 controller features a HV startup current source that allows fast startup time and extremely low standby power consumption. Two startup current levels (I_{start1} and I_{start2}) are provided by the system for safety in case of short circuit between VCC and GND pins. In addition, the HV startup current source features a dedicated over−temperature protection to prevent IC damage for any failure mode that may occur in the application. The HV startup current source is primarily enabled or disabled based on V_{CC} level. The startup HV current source can be also enabled by BO_OK rising edge, auto−recovery timer end, REMote and TSD end event. The HV startup current source charges the VCC capacitor before IC start−up.

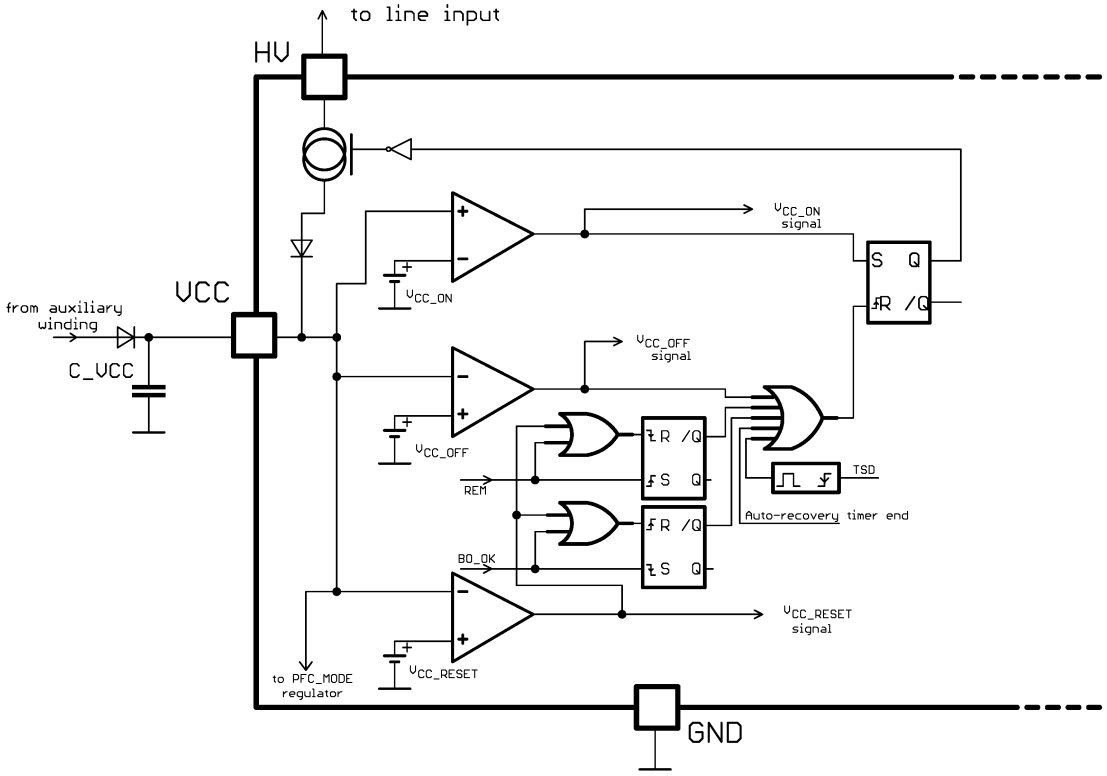


Figure 37. Internal Connection of the VCC Management Block

The NCP1399 controller disables the HV startup current source once the VCC pin voltage level reaches V_{CC_ON} threshold – refer to Figure 37. The application then starts operation and the auxiliary winding maintains the voltage bias for the controller during normal and skip−mode operating modes. The IC operates in so called Dynamic Self Supply (DSS) mode when the bias from auxiliary winding is not sufficient to keep the V_{CC} voltage above V_{CC_OFF} threshold (i.e. V_{CC} voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds with no driver pulses on the output during positive V_{CC} ramp). The HV source is also operated in DSS mode when the low voltage controller enters off−mode or fault−mode operation. In this case the VCC pin voltage will cycle between V_{CC_ON} and V_{CC_OFF} thresholds and the controller will not deliver any driver pulse – waiting for return from the off−mode or latch mode operation. Please refer to figures Figure 61 through Figure 65 to find an illustration of the NCP1399 VCC management system under all operating conditions/modes.

The HV startup current source features an independent over−temperature protection system to limit I_{start2} current when the die temperature reaches 130°C. At this temperature, I_{start2} will be progressively to prevent the die temperature from rising above 130°C.

Brown−out Protection − VBULK/PFC FB Input

Resonant tank of an LLC converter is always designed to operate within a specific bulk voltage range. Operation below minimum bulk voltage level would result in current and temperature overstress of the converter power stage. The NCP1399 controller features a VBULK/PFC FB input in order to precisely adjust the bulk voltage turn−ON and turn−OFF levels. This Brown−Out protection (BO) greatly simplifies application level design.

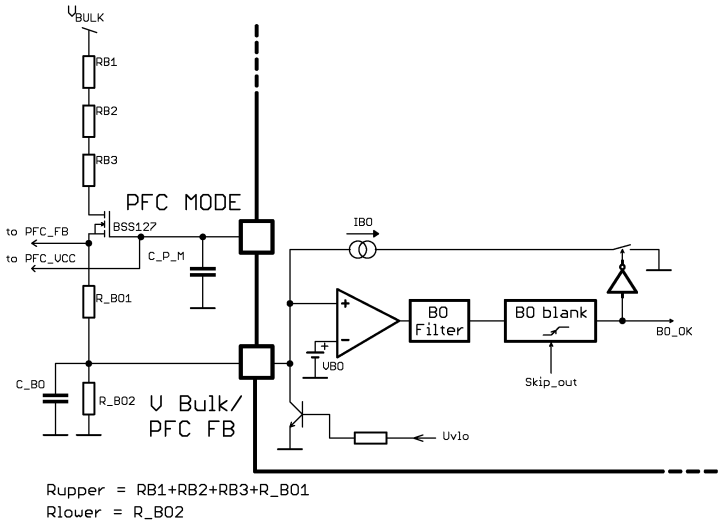


Figure 38. Internal Connection of the Brown−out Protection Block

The internal circuitry shown in Figure 38 allows monitoring the high−voltage input rail (V_{bulk}). A high−impedance resistive divider made of R_{upper} and R_{lower} resistors brings a portion of the V_{bulk} rail to the VBULK/PFC FB pin. The Current sink (I_{BO}) is active below the bulk voltage turn−on level (V_{bulk_ON}). Therefore, the bulk voltage turn−on level is higher than defined by the division ratio of the resistive divider. To the contrary, when the internal BO_OK signal is high, i.e. the application is running, the I_{BO} sink is disabled. The bulk voltage turn−off threshold (V_{bulk_OFF}) is then given by BO comparator reference voltage directly on the resistor divider. The advantage of this solution is that the V_{bulk_OFF} threshold precision is not affected by I_{BO} hysteresis current sink tolerance.

The V_{bulk_ON} and V_{bulk_OFF} levels can be calculated using equations below:

The I_{BO} is ON:

$$V_{BO} + V_{BOhyst} = V_{bulk_ON} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 1)}$$

The I_{BO} is OFF:

$$V_{BO} = V_{bulk_OFF} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

One can extract R_{lower} term from equation 2 and use it in equation 1 to get needed R_{upper} value:

$$R_{lower} = \frac{\frac{V_{bulk_ON} \cdot V_{BO}}{V_{bulk_OFF}} - V_{BO} - V_{BOhyst}}{I_{BO} \cdot \left(1 - \frac{V_{BO}}{V_{bulk_OFF}} \right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk_OFF} - V_{BO}}{V_{BO}} \quad \text{(eq. 4)}$$

Note that the VBULK/PFC FB pin is pulled down by an internal switch when the controller is in startup phase – i.e. when the V_{CC} voltage ramps up from $V_{CC} < V_{CC_RESET}$ towards the V_{CC_ON} level on the VCC pin. This feature assures that the VBULK/PFC FB pin voltage will not ramp up before the IC operation starts. The I_{BO} hysteresis current sink is activated and BO discharge switch is disabled once the V_{CC} voltage crosses V_{CC_ON} threshold. The VBULK/PFC FB pin voltage then ramps up naturally according to the BO divider information. The BO comparator then authorizes or disables the LLC stage operation based on the actual V_{bulk} level.

The low I_{BO} hysteresis current of the NCP1399 brown out protection system allows increasing the bulk voltage divider resistance and thus reduces the application power consumption during light load operation. On the other hand, the high impedance divider can be noise sensitive due to capacitive coupling to HV switching traces in the application. This is why a filter (t_{BO_FILTR}) is added after the BO comparator in order to increase the system noise immunity. Despite the internal filtering, it is also recommended to keep a good layout for BO divider resistors and use a small external filtering capacitor on the VBULK/PFC pin if precise BO detection wants to be achieved.

The bulk voltage HV divider can be also used by a PFC front stage controller as a feedback sensing network (refer again to Figure 38). The shared bulk voltage resistor divider between PFC and LLC stage offers a way how to further reduce power losses during off−mode and no−load operation. The NCP1399 features a PFC MODE pin that disconnects bias of the PFC stage during light load, off−mode or fault mode operation. The signal from the PFC MODE pin can be also used to control an external HV switch in order to disconnect the bulk voltage divider from bulk during off−mode operation. This technique further reduces

the no−load power consumption down again since the power losses of voltage divider are not affected by the bulk voltage at all.

Please refer to Figure 61 through Figure 65 for an illustration of NCP1399 Brown−out protection system in all operating conditions/modes.

Over−voltage and Over−temperature Protection

The OVP/OTP pin is a dedicated input to allow for a simple and cost effective implementation of two key protection features that are needed in adapter applications: over−voltage (OVP) and over−temperature (OTP) protections. Both of these protections can be either latched or auto−recovery– depending on the version of NCP1399. The OVP/OTP pin has two voltage threshold levels of detection (V_{OVP} and V_{OTP}) that define a no−fault window. The controller is allowed to run when OVP/OTP input voltage is within this working window. The controller stops the operation, after filter time delay, when the OVP/OTP input voltage is out of the no−fault window. The controller then either latches−off or or starts an auto−recovery timer – depending on the IC version – and triggered the protection threshold (V_{OTP} or V_{OVP}).

The internal current source I_{OTP} allows a simple OTP implementation by using a single negative temperature coefficient (NTC) thermistor. An active soft clamp composed from V_{clamp} and R_{clamp} components prevents the OVP/OTP pin voltage from reaching the V_{OVP} threshold when the pin is pulled up by the I_{OTP} current. An external pull−up current, higher than the pull − down capability of the internal clamp ($V_{CLAMP_OVP/OTP}$), has to be applied to pull the OVP/OTP pin above V_{OVP} threshold to activate the OVP protection. The t_{OVP_FILTER} and t_{OTP_FILTER} filters are implemented in the system to avoid any false triggering of the protections due to application noise and/or poor layout.

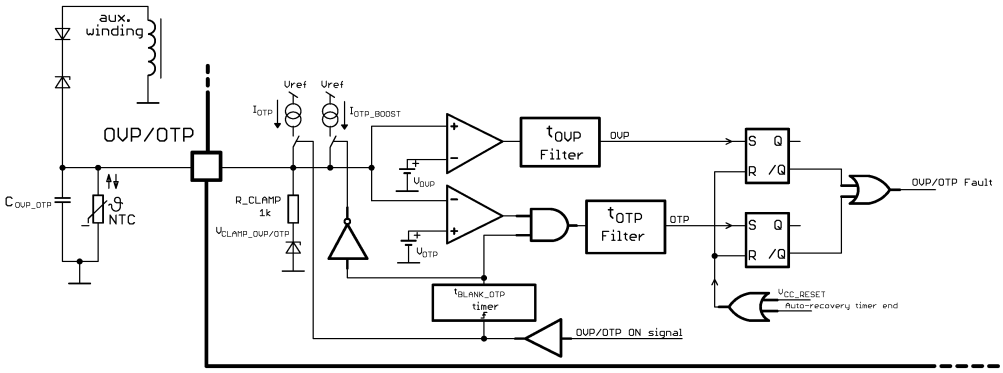


Figure 39. Internal Connection of OVP/OTP Input

The OTP protection could be falsely triggered during controller startup due to the external filtering capacitor charging current. Thus the t_{BLANK_OTP} period has been implemented in the system to overcome such behavior. The OTP comparator output is ignored during t_{BLANK_OTP} period. In order to speed up the charging of the external filtering capacitor C_{OVP_OTP} connected to OVP/OTP pin, the I_{OTP} current has been doubled to I_{OTP_BOOST}. The maximum value of filtering capacitor is 47 nF.

The OVP/OTP ON signal is set after the following events:

- the V_{CC} voltage exceeds the V_{CC_ON} threshold during first start−up phase (after VCC pin voltage was below V_{CC_RESET} threshold)
- BO OK signal is received from BO block
- Auto−recovery timer elapsed and a new restart occurs
- IC returns to operation from skip−mode ($V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold was reached)
- IC returns to operation from off−mode (V_{REM_ON} or $V_{FB_REM_ON}$ signal is received by off−mode control block)

The I_{OTP} current source is disabled when:

- V_{CC} falls below V_{CC_OFF} threshold
- BO OK signal goes to low state (i.e. Brown−out condition occurs on the mains)
- Fault signal is activated (Auto−recovery timer starts counting or Latch fault is present)
- IC goes into the skip−mode operation ($V_{FB_SKIP_IN}$ threshold was reached)
- IC goes into the off−mode operation (V_{REM_OFF} or ($V_{FB_REM_OFF}$ & V_{CC_OFF}) signal was reached)

The latched OVP or OTP versions of NCP1399 enters latched protection mode when V_{CC} voltage cycles between V_{CC_ON} and V_{CC_OFF} thresholds and no pulses are provided by drivers. The controller VCC pin voltage has to be cycled down below V_{CC_RESET} threshold in order to restart operation. This would happen when the power supply is unplugged from the mains.

SKIP/REM Input and Off−mode Control

The NCP1399 implements an ultra−low power consumption mode of operation called off−mode. The application output voltage is cycled between the nominal and lower levels that are defined by the secondary side off−mode controller (like NCP435x secondary off−mode controller). The output voltage is thus not regulated to nominal level but is always kept at a high enough voltage level to provide bias for the necessary circuits in the target application – for example this could be the case of microcontroller with very low consumption that handles VCC management in a notebook or TV. The no−load input power consumption could be significantly reduced when using described technique. The NCP1399 implements two different off−mode control system approaches:

- Active ON off−mode control – available on the NCP1399By device family
- Active OFF off−mode control – available on the NCP1399Ay device family

These two off−mode operation control techniques differ in the way the off−mode operation is started on the primary side controller. Both of these methods are described separately hereinafter.

Active ON Off−mode Control – NCP1399B Device Family

The NCP1399B device family uses a SKIP/REM pin only for off−mode operation control– i.e. the pin is internally connected to the Active ON off−mode control block and the skip mode threshold level is not adjustable externally. The skip mode comparator threshold can be adjusted only internally (by IC option) in this package option. The SKIP/REM pin when used for off−mode control allows the user to activate the ultra−low consumption mode during which the IC consumption is reduced to only very low HV pin leakage current ($I_{HV_OFF−MODE}$) and very low VCC pin consumption ($I_{CC_OFF−MODE}$). The off − mode is activated when SKIP/REM pin voltage exceeds V_{REM_OFF} threshold. Normal operating mode is resumed when SKIP/REM pin voltage drops below V_{REM_ON} threshold – refer to Figure 40 for an illustration.

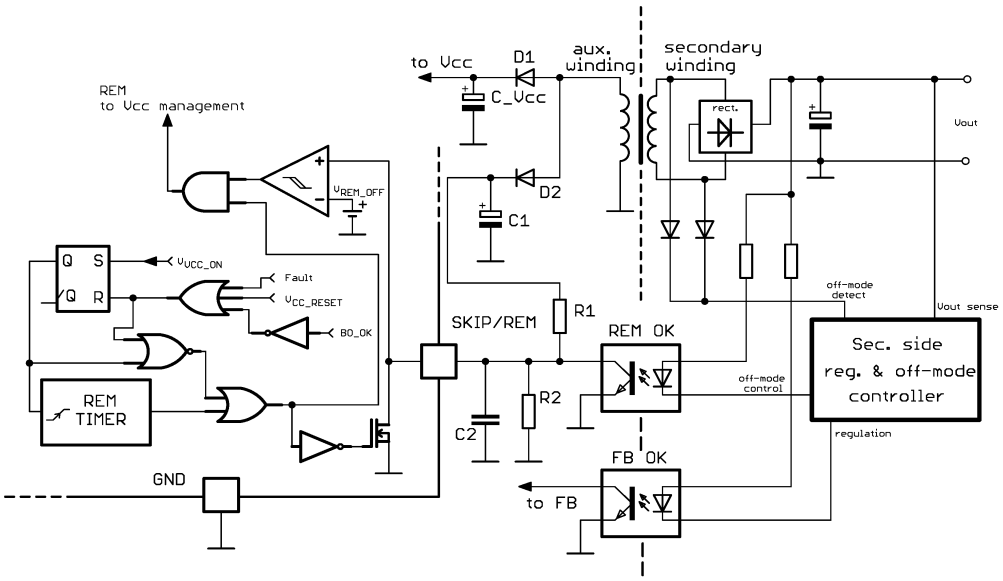


Figure 40. SKIP/REM Input Internal Connection – Active ON Version

The off−mode operation is activated by the secondary side off−mode controller. The auxiliary bias for primary side off−mode control is provided by a circuit composed from components D_2, C_1, R_1, R_2 and C_2. The SKIP/REM pin is pulled up by this auxiliary supply circuit once the REM optocoupler (REM OK) is released. The application then operates in off−mode until the secondary side off−mode controller activates the REM optocoupler or until the auxiliary bias on C_1 is lost. Normal operation mode is then recovered via power stage startup. The application is thus switching between ON−mode and OFF−mode states when off−mode control is implemented. The OFF mode period last significantly longer time (tens of seconds or more) compared to the secondary capacitor refilling period (few tens of milliseconds) – this explains why the no−load input power consumption can be drastically reduced. The auxiliary off−mode supply capacitor C1 can stay charged while the secondary bias is lost – this can happen during overload or other fault mode conditions. A REM TIMER is thus implemented in the system to allow fast application

restart in such cases. The controller blanks the SKIP/REM input information and pulls down the SKIP/REM input for t_{REM_TIMER} time during controller restart so that the secondary side bias can be restored and the secondary off−mode controller can activate the REM optocoupler. This REM TIMER blank sequence is activated each time the VCC pin voltage reaches V_{CC_ON} threshold – except in the situation when after IC left off−mode operation by standard way and V_{CC} is restored – i.e. when the REM optocoupler is activated by the secondary off−mode controller.

The SKIP/REM input blanking is activated in following cases:

- VCC pin voltage reaches V_{CC_ON} threshold during first start−up phase (i.e. when V_{CC} was below V_{CC_RESET} threshold before)
- Auto−recovery timer elapsed and new start is initiated

The REM TIMER helps to assure fast application re−start from fault conditions by forcing controller operation after t_{REM_TIMER} . However, the secondary controller drives the remote pin via REM optocoupler during normal operating conditions in order to switch between ON and OFF operating modes. The controller is active for very short time during no−load conditions – just during the time needed to re−fill the secondary side capacitors to the nominal output voltage level. In this case we do not use REM TIMER because it would increase the no−load power consumption by forcing the application to run for a longer time than necessary. The REM TIMER blank period is thus not activated in no−load conditions.

The bias on VCC pin needs to be assured when off−mode operation takes place. The auxiliary winding is no more able to provide any bias thus the HV startup current source is operated in DSS mode – i.e. the VCC pin voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds. This approach keeps IC biasing in order to memorize the current operation sate.

Please refer to Figure 64 for an illustration on how the NCP1399 Active ON off−mode system works under all operating conditions/modes.

Active OFF Off−mode Control – NCP1399A Device Family

The NCP1399A device family uses LLC FB pin voltage information for off−mode operation detection – refer to Figure 41. The SKIP/REM pin is internally connected to the skip mode block in this case and serves as a $V_{FB_SKIP_IN}$ threshold voltage adjust pin. The secondary off−mode controller reuses the LLC stage regulation optocoupler in order to reduce total system cost. The off−mode operation is initiated once the LLC FB pin is pulled down below V_{REM_ON} threshold and the VCC pin voltage drops below V_{CC_OFF} threshold in the same time. The optocoupler has to be active at all time the application is held in off−mode. No biased is then provided by the secondary off−mode controller during normal operation – this is why this approach is called Active OFF off−mode operation. The application no−load input power consumption is slightly higher compared to Active ON off−mode solution, previously described, because the optocoupler needs to be biased during off mode operation

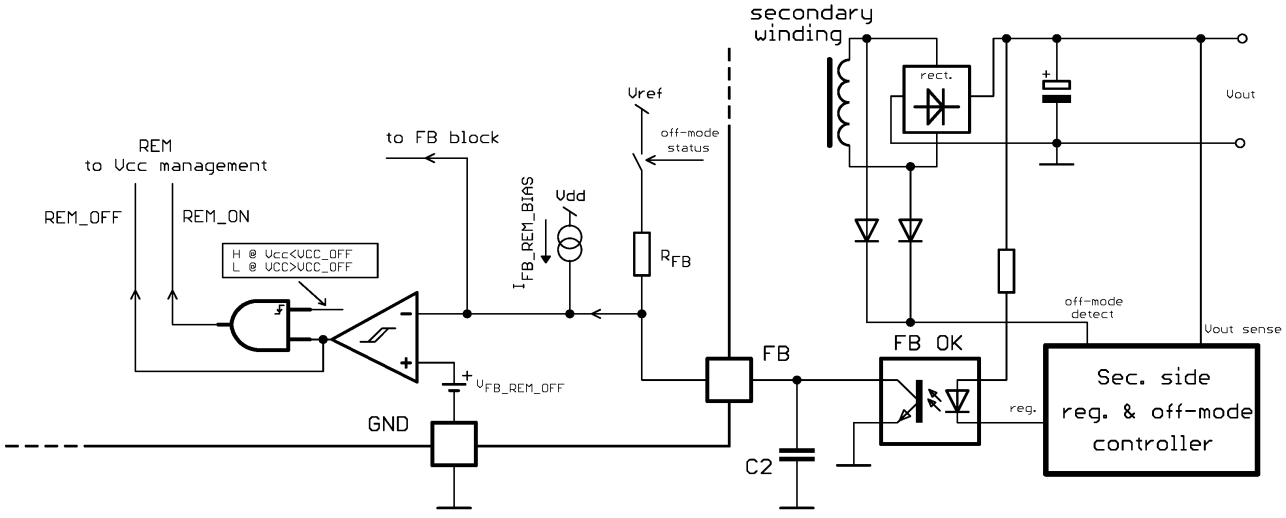


Figure 41. Active OFF Off−mode Internal Detection Based on the LLC FB Pin Voltage

The controller monitors the LLC FB pin voltage level and restarts via regular startup sequence (including VCC pin voltage ramp−up to V_{CC_ON} level and soft−start) once the FB pin is released by the secondary off−mode controller.

The HV startup current source is working in DSS mode during application off−mode operation – i.e. the VCC pin voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds. This approach keeps IC biased so that the actual operation sate is memorized. The LLC FB pin pull−up resistor is disconnected when off−mode operation is activated in order to reduce IC power consumption and also needed current for optocoupler driving from secondary side.

Please refer to Figure 65 for an illustration on how the NCP1399 active ON off−mode system works under all operating conditions/modes.

PFC MODE Output and P ON/OFF Control Pin

The NCP1399 has two pins P ON/OFF and PFC MODE that can be used to disable or enable PFC stage operation based on actual application operating state – please refer to Figure 46. The PFC MODE pin voltage is changed ($V_{PFC_M_ON}$ or $V_{PFC_M_BO}$) based on the actual P ON/OFF input logic signal state. Minimum impedance connected to P ON/OFF pin is 1 kΩ. The PFC stage operation can thus be disabled/enabled via external logic signal. This option should be used with the wide range input voltage LLC tank designed to assure correct operation of the LLC stage through whole bulk voltage range. The PFC MODE output pin can be used for two purposes:

1. to control the external small signal HV MOSFET switch that connects the bulk voltage divider to the VBULK/PFC FB input
2. to control the PFC front stage controller operation via PFC controller supply pin

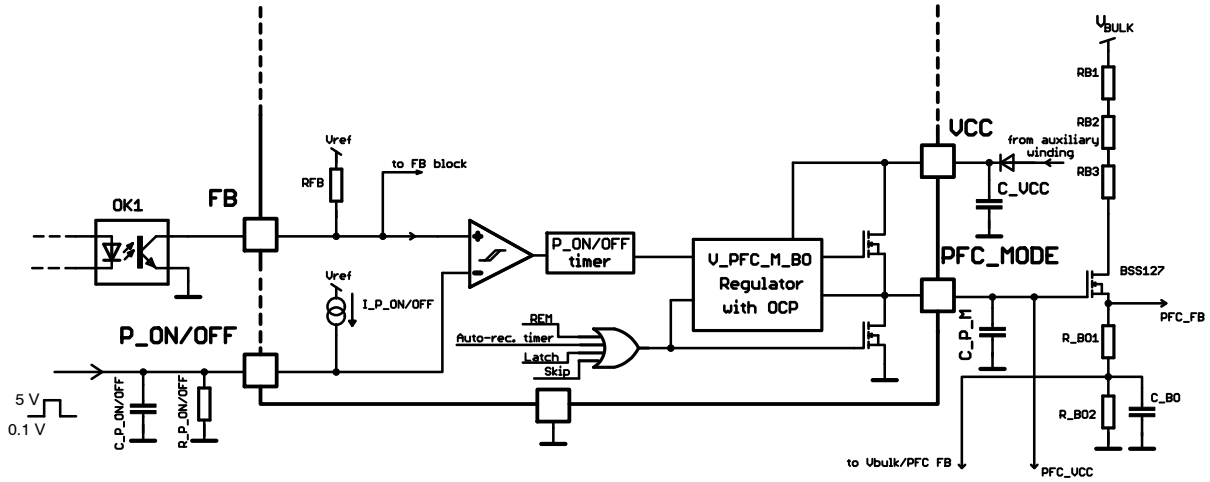


Figure 42. Internal Connection of the PFC MODE and P ON/OFF Blocks

There are three possible states of the PFC MODE output that can be placed by the controller based on the application operating conditions:

1. The PFC MODE output pin is pulled−down by an internal MOSFET switch before controller startup. This technique ensures minimum VCC pin current consumption in order to ramp V_{CC} voltage in a short time from the HV startup current source which speeds up the startup or restart process. The PFC MODE output pin is also pulled−down in off−mode or protection mode during which the HV startup current source is operated in DSS mode. This reduces the application power consumption in both cases.
2. The pull−down switch is disabled and the internal regulator enabled by the controller to provide $V_{PFC_M_BO}$ reference when an external logic signal on the P ON/OFF pin is at “high” state. An internal regulator includes current limitation for the PFC MODE output that is set to $I_{PFC_M_LIM}$ when $V_{PFC_M_BO}$ reference is provided. The PFC MODE pin drives external small signal HV MOSFET switch to keep bulk voltage divider connected. The LLC power stage Brown−out protection system thus works when the LLC stage is switching while PFC stage disabled.
3. The pull−down switch is disabled and the internal regulator is switched to bypass mode in which it connects VCC pin voltage to PFC MODE output with minimum dropout ($V_{PFC_M_ON}$). This state of the PFC MODE output appears in case an external signal on the P ON/OFF pin is at “low” state.

The output power level is derived internally from the actual FB pin voltage. This information could be compared on external comparator with the reference level and control the P ON/OFF input, thus the user has possibility to adjust power below which the PFC stage is disabled in order to increase efficiency in light load conditions. The P ON/OFF comparator features an hysteresis ($P\ ON/OFF_{HYST}$) proportional to the set P ON/OFF level in order to overcome PFC power stage oscillations (periodical ON/OFF operation). The P ON/OFF timer ($t_{P\ ON/OFF_TIMER}$) is implemented to ensure a long enough propagation delay from the PFC turn OFF detection to PFC MODE output deactivation. This timer is unidirectional so that it resets immediately after PFC ON condition is detected by the P ON/OFF comparator. This technique is used in order to avoid a PFC stage deactivation during load or line transients. The PFC MODE pin output current is limited when the VCC to PFC MODE bypass switch is activated. The current limitation avoids bypass switch damage during PFC VCC decoupling capacitor charging process or short circuit. A minimum value PFC VCC decoupling capacitance should be used in order to speed up PFC stage startup after it is enabled by the NCP1399 controller.

Please refer to Figure 61 through Figure 65 for an illustration of NCP1399 PFC operation control.

ON−time Modulation and Feedback Loop Block

Frequency modulation of today's commercially available resonant mode controllers is based on the output voltage regulator feedback only. The feedback voltage (or current) of output regulator drives voltage (or current) controlled oscillator (VCO or CCO) in the controller. This method presents three main disadvantages:

1. The 2nd order pole is present in small signal gain−phase characteristics ≥ the lower cross over frequency and worse transient response is imposed by the system when voltage mode control is used. There is no direct link to the actual primary current – i.e. no line feed forward mechanism which results in poor line transient response.
2. Precise VCO (or CCO) is needed to assure frequency modulation with good reproducibility, f_{min} and f_{max} clamps need to be adjusted for each design ≥ need for an adjustment pin(s).
3. Dedicated overload protection system, requiring an additional pin, is needed to assure application safety during overload and/or secondary short circuit events.

The NCP1399 resolves all disadvantages mentioned above by implementing a current mode control scheme that ensures best transient response performance and provides inherent cycle−by−cycle over−current protection feature in the same time. The current mode control principle used in this device can be seen in Figure 43.

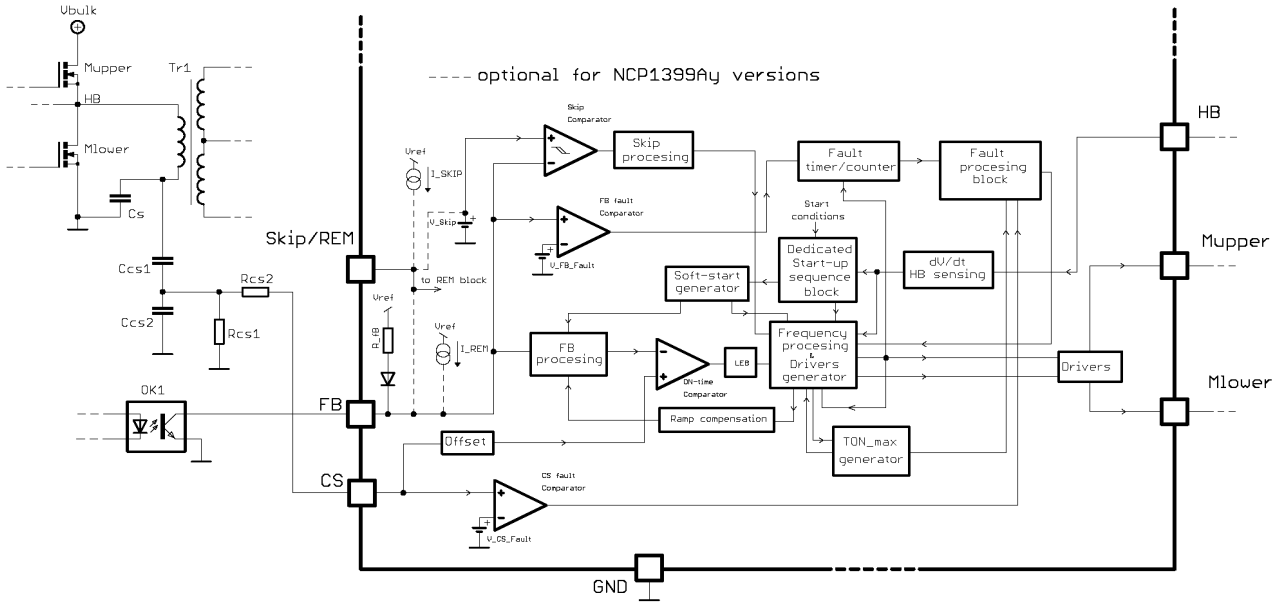


Figure 43. Internal Connection of the NCP1399 Current Mode Control Scheme

The basic principle of current mode control scheme implementation lies in the use of an ON−time comparator that defines upper switch on−time by comparing voltage ramp, derived from the current sense input voltage, to the divided feedback pin voltage. The upper switch on−time is then re−used for low side switch conduction period. The switching frequency is thus defined by the actual primary current and output load conditions. Digital processing with 10 ns minimum on−time resolution is implemented to ensure high noise immunity. The ON−time comparator output is blanked by the leading edge blanking (t_{LEB}) after the Mupper switch is turned−on. The ON−time comparator LEB period helps to avoid false triggering of the on−time modulation due to noise generated by the HB pin voltage transition.

The voltage signal for current sense input is prepared externally via natural primary current integration by the resonant tank capacitor Cs. The resonant capacitor voltage is divided down by capacitive divider (Ccs1, Ccs2, Rcs1, Rcs2) before it is provided to the CS input. The capacitive divider division ratio, which is fully externally adjustable, defines the maximum primary current level that is reached in case of maximum feedback voltage – i.e. the capacitive divider division ration defines the maximum output power of the converter for given bulk voltage. The CS is a bipolar input pin which an input voltage swing is restricted to ±5 V. A fixed voltage offset is internally added to the CS pin signal in order to assure enough voltage margin for operation the feedback optocoupler – the FB optocoupler saturation voltage is ~ 0.15 V (depending on type). However, the CS pin useful signal for frequency modulation swings from 0 V, so current mode regulation would not work under light load conditions if no offset would be added to the CS pin before it is stabilized to the level of the on−time comparator input. The CS pin signal is also used for secondary side short circuit detection – please refer to chapter dedicated to short circuit protection.

The second input signal for the on−time comparator is derived from the FB pin voltage. This internal FB pin signal is also used for the following purposes: skip mode operation detection, PFC MODE control, off−mode detection (in NCP1399A device family) and overload / open FB pin fault detection. The detailed description of these functions can be found in each dedicated chapters. The internal pull−up resistor assures that the FB pin voltage increases when the optocoupler LED becomes less biased – i.e. when output load is increased. The higher FB pin voltage implies a higher reference level for on−time comparator i.e. longer Mupper switch on−time and thus also higher output power. The FB pin features a precise voltage clamp which limits the internal FB signal during overload and startup. The FB pin signal passes through the FB processing block before it is brought to the ON−time comparator input. The FB processing block scales the FB signal down by a K_{FB} ratio in order to limit the CS input dynamic voltage range. The scaled FB signal is then further processed by subtraction of a ramp compensation generator signal in order to ensure stability of the current mode control scheme. The divided internal FB signal is overridden by a Soft−start generator output voltage during device starts−up.

The actual operation frequency of the converter is defined based on the CS pin and FB pin input signals. Please refer to Figure 44 and below description for better understanding of the NCP1399 frequency modulation system.

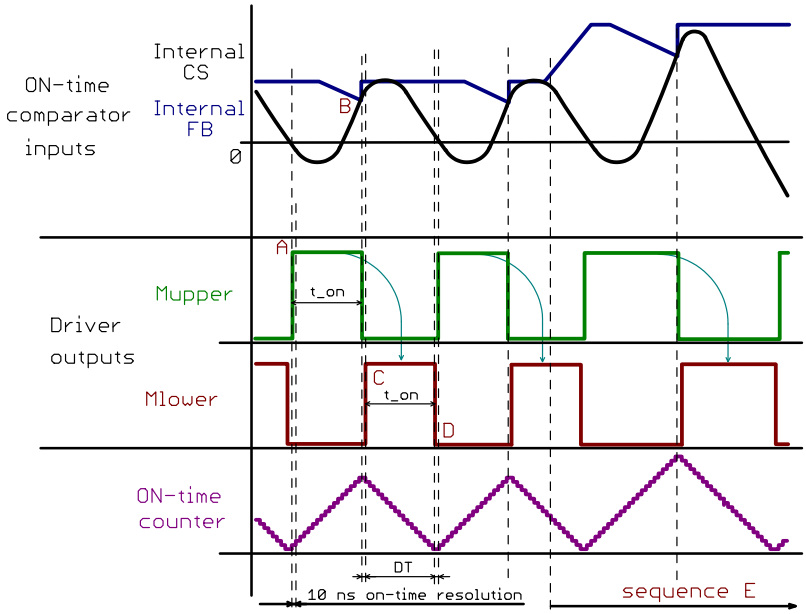


Figure 44. NCP1399 On−time Modulation Principle

The Mupper switch is activated by the controller after dead−time (DT) period lapses in point **A**. The frequency processing block increments the ON−time counter with 10 ns resolution until the internal CS signal crosses the internal FB set point for the ON−time comparator in point **B**. A DT period is then introduced by the controller to avoid any shoot−through current through the power stage switches. The DT period ends in point **C** and the controller activates the Mlower switch. The ON−time processing block decrements the ON_time counter down until it reaches zero. The Mlower switch is then turned−OFF at point **D** and the DT period is started. This approach results in perfect duty cycle symmetry for Mlower and Mupper switches. The Mupper switch on−time naturally increases and the operating frequency drops when the FB pin voltage is increased, i.e. when higher current is delivered by the converter output – sequence **E**.

The resonant capacitor voltage and thus also CS pin voltage can be out of balance in some cases – this is the case during transition from full load to no−load operation when skip mode is not used or adjusted correctly. The current mode operation is not possible in such case because the ON−time comparator output stays active for several switching cycles. Thus a special logic has been implemented in NCP1399 in order to repeat the last valid on−time until the current mode operation recovers – i.e. until the CS pin signal balance is restored by the system.

Overload and Open FB Protections

The overload protection and open FB pin detection are implemented via FB pin voltage monitoring in this controller. The FB fault comparator is triggered once the FB pin voltage reaches its maximum level and the V_{FB_FAULT} threshold is exceeded. The fault timer or counter (depending on IC option) is then enabled – refer to Figure 43. The time period to the FB fault event confirmation is defined by the preselected $t_{FB_FAULT_TIMER}$ parameter when the fault timer option is used. The FB fault counter, once selected as a FB fault confirmation period source, defines the fault confirmation period via Mupper DRV pulses counting. The

FB fault confirmation time is thus dependent on switching frequency. The fault timer/counter is reset once the FB fault condition diminishes. A digital noise filter has been added after the FB fault comparator to overcome false triggering of the FB fault timer/counter due to possible noise on the FB input. The noise filter has a period of 2 μs for FB fault timer/counter activation and 20 μs for reset/deactivation to assure high noise immunity. A cumulative timer/counter IC option is also available on request. The FB fault timer/counter is not reset when the FB fault condition diminishes in this case. The FB fault timer/counter is disabled and memorizes the fault period information. The cumulative FB fault timer/counter integrates all the FB fault events over the IC operation time. The Fault timer/counter can be reset via skip mode or VCC UVLO event.

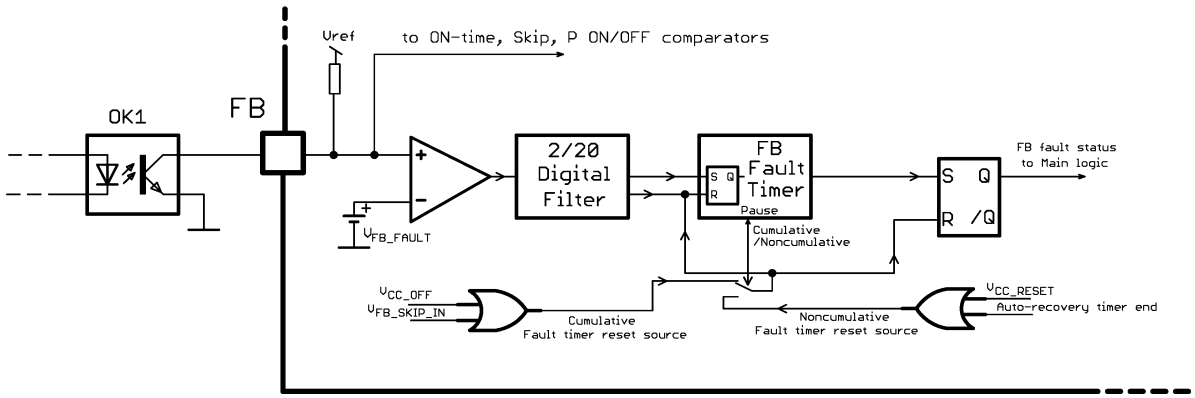


Figure 45. Internal FB Fault Management

The controller disables driver pulses and enters protection mode once the FB fault event is confirmed by the FB fault timer or counter. Latched or auto−recovery operation is then triggered – depends on selected IC option. The controller adds an auto−recovery off−time period (t_{A-REC_TIMER}) and restarts the operation via soft start in case of auto−recovery option. The application temperature runaway is thus avoided in case of overload while the automatic restart is still possible once the overload condition disappears. The IC with latched FB fault option stays latched−off, supplied by the HV startup current source working in DSS mode, until the V_{CC_RESET} threshold is reached on the VCC pin – i.e. until user re−connects power supply mains.

Please refer to Figure 61 and Figure 62 for an illustration of the NCP1399 FB fault detection block.

Secondary Short Circuit Detection

The protection system described previously, implemented via FB pin voltage level detection, prevents continuous overload operation and/or open FB pin conditions. The primary current is naturally limited by the NCP1399 on−time modulation principle in this case. But the primary current increases when the output terminals are shorted. The NCP1399 controller will maintain zero voltage switching operation in such case, however high currents will flow through the power MOSFETS, transformer winding and secondary side rectification. The NCP1399 implements a dedicated secondary side short circuit protection system that will shut down the controller much faster than the regular FB fault event in order to limit the stress of the power stage components. The CS pin signal is monitored by the dedicated CS fault comparator − refer to Figure 43. The CS fault counter is incremented each time the CS fault comparator is triggered. The controller enters auto−recovery or latched protection mode (depending on IC option) in case the CS fault counter overflows refer to Figure 46. The CS fault counter is then reset once the CS fault comparator is inactive for at least 50 Mupper upcoming pulses. This digital filtering improves CS fault protection system noise immunity.

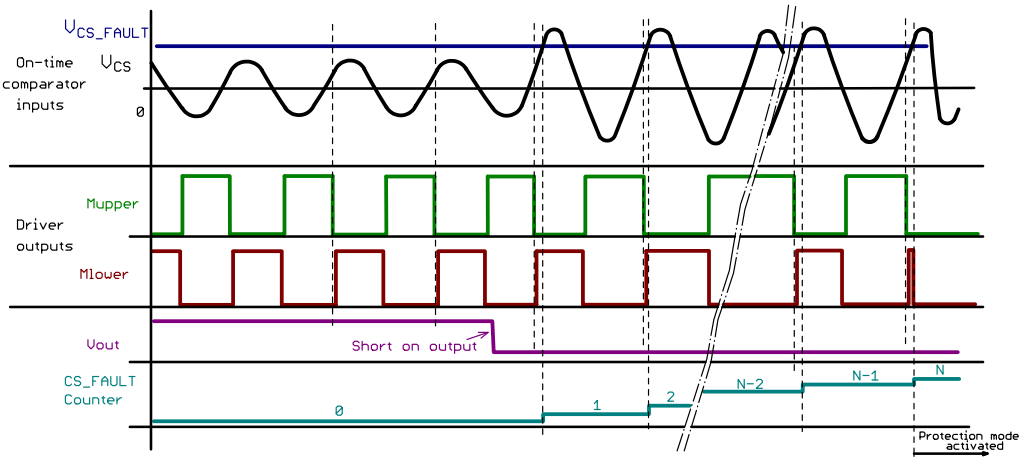


Figure 46. NCP1399 CS Fault Principle

Dedicated Startup Sequence and Soft−Start

Hard switching conditions can occur in a resonant SMPS application when the resonant tank operation is started with 50% duty cycle symmetry – refer to Figure 47. This hard switching appears because the resonant tank initial conditions are not optimal for the clean startup.

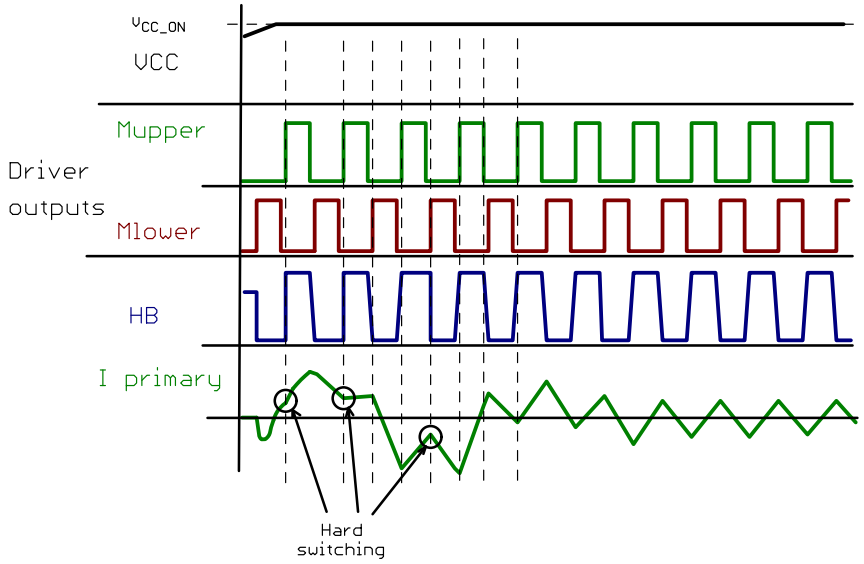


Figure 47. Hard switching cycle appears in the LLC application when resonant tank is excited by 50% duty cycle during startup

The initial resonant capacitor voltage level can differ depending on how long delay was placed before application operation restart. The resonant capacitor voltage is close to zero level when application restarts after very long delay – for example several seconds, when the resonant capacitor is discharged by leakage to the power stage. However, the resonant capacitor voltage value can be anywhere between Vbulk and 0 V when the application restarts operation after a short period of time – like during periodical SMPS turn−on/off. Another factor that plays significant role during resonant power supply startup is the actual load impedance seen by the power stage during the first pulses of startup sequence. This impedance is not only defined by resonant tank components but also by the output loading conditions and actual output voltage level. The load impedance of resonant tank is low when the output is loaded and/or the output voltage is low enough to made secondary rectifies conducting during first switching cycles of startup phase. The resonant frequency of the resonant tank is given by the resonant capacitor capacitance and resonant inductance −note that the magnetizing inductance does not participate in resonance in this case. However, if the application starts−up when the output capacitors is charged and there is no load connected to the output, the secondary rectification diodes is not conducting during each switching cycle of startup sequence and thus the resonant frequency of resonant tank is affected also by the magnetizing inductance. In this case, the resonant frequency is much lower than in case of startup into loaded/discharged output.

These facts show that a clean, hard switching free and parasitic oscillation free, startup of an LLC converter is not an easy task, and cannot be achieved by duty cycle imbalance and/or simple resonant capacitor pre−charge to Vbulk/2 level. These methods only work in specific startup conditions.

This explains why the NCP1399 implements a proprietary startup sequence − see Figure 48 and Figure 49. The resonant capacitor is discharged down to 0 V before any application restart − except when restarting from skip mode.

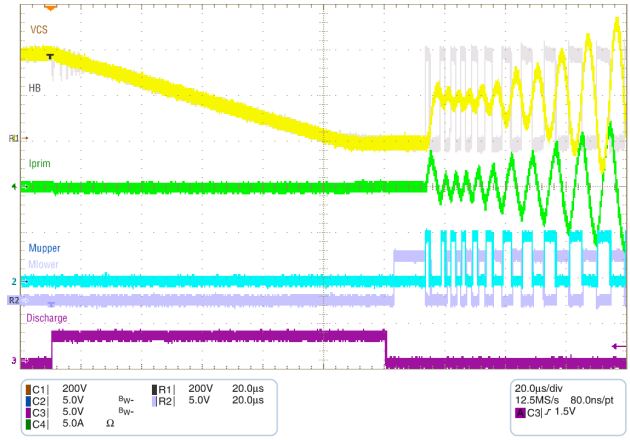


Figure 48. Initial Resonant Capacitor Discharge before Dedicated Startup Sequence is Placed

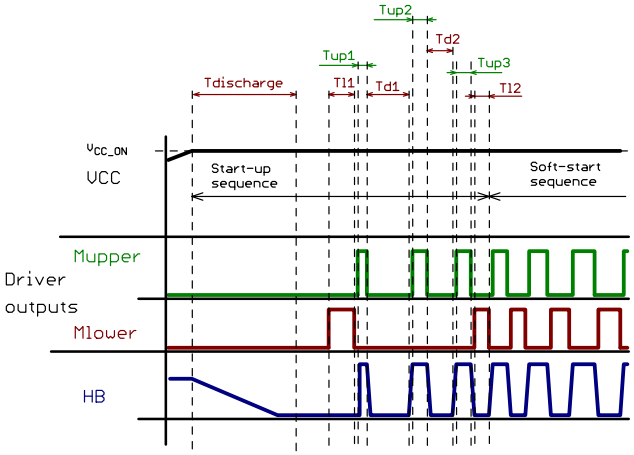


Figure 49. Dedicated Startup Sequence Detail

The resonant capacitor discharging process is simply implemented by activating an internal current limited switch connected between the HB pin and IC ground − refer to Figure 48. This technique assures that the resonant capacitor energy is dissipated in the controller without ringing or oscillations that could swing the resonant capacitor voltage to a positive or negative level. The controller detects that the discharge process is complete via HB pin voltage level monitoring. The discharge switch is disabled once the HB pin voltage drops below the V_{HB_MIN} threshold.

The dedicated startup sequence continues by activation of the Mlower driver output for Tl1 period (refer to Figure 49). This technique ensures that the bootstrap capacitor is fully charged before the first high−side driver pulse is introduced by the controller. The first Mupper switch on−time Tup1 period is fixed and depends on the application parameters. This period can be adjusted internally − various IC options are available. The Mupper switch is released after T_{up1} period and it is not followed by the Mlower switch activation. The controller waits for a new ZVS condition for Mupper switch instead and measures actual resonant tank conditions this way. The Mupper switch is then activated again after the Mlower blank period is used for measurment purposes. The second Mupper driver conduction period is then dependent on the previously measured conditions:

1. The Mupper switch is activated for 3/2 of previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is twice higher than the the previous Mupper pulse conduction period
2. The Mupper switch is activated for previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is twice lower than the previous Mupper pulse conduction period

The startup period then depends on the previous condition. Another blank Mlower switch period is placed by the controller in case condition 1 occurred. A normal Mlower driver pulse, with DC of 50% to previous Mupper DRV pulse, is placed in case condition 2 is fulfilled.

The dedicated startup sequence is placed after the resonant capacitor is discharged (refer to Figure 48 and Figure 49) in order to exclude any hard switching cycles during the startup sequence. The first Mupper switch cycle in startup phase is always non−ZVS cycle because there is no energy in the resonant tank to prepare ZVS condition. However, there is no energy in the resonant tank at this time, there is also no possibility that the power stage MOSFET body diodes conducts any current. Thus the hard commutation of the body diode cannot occur in this case.

The IC will not start and provide regular driver output pulses until it is placed into the target application, because the startup sequence cannot be finished until HB pin signal is detected by the system. The IC features a startup watchdog timer ($t_{WATCHDOG}$) which activates a dedicated startup sequence periodically in case the IC is powered without application (during bench testing) or in case the startup sequence is not finished correctly. The IC will provide the first Mlower and first Mupper DRV pulses with a $t_{WATCHDOG}$ off−time in−between startup attempts.

Soft−start

The dedicated startup sequence is complete when condition 2 from previous chapter is fulfilled and the controller continues operation with the soft−start sequence. A fully digital non−linear soft−start sequence has been implemented in NCP1399 using a soft−start counter and D/A converter that are gradually incremented by the Mlower driver pulses. A block diagram of the NCP1399 soft−start system is shown in Figure 50.

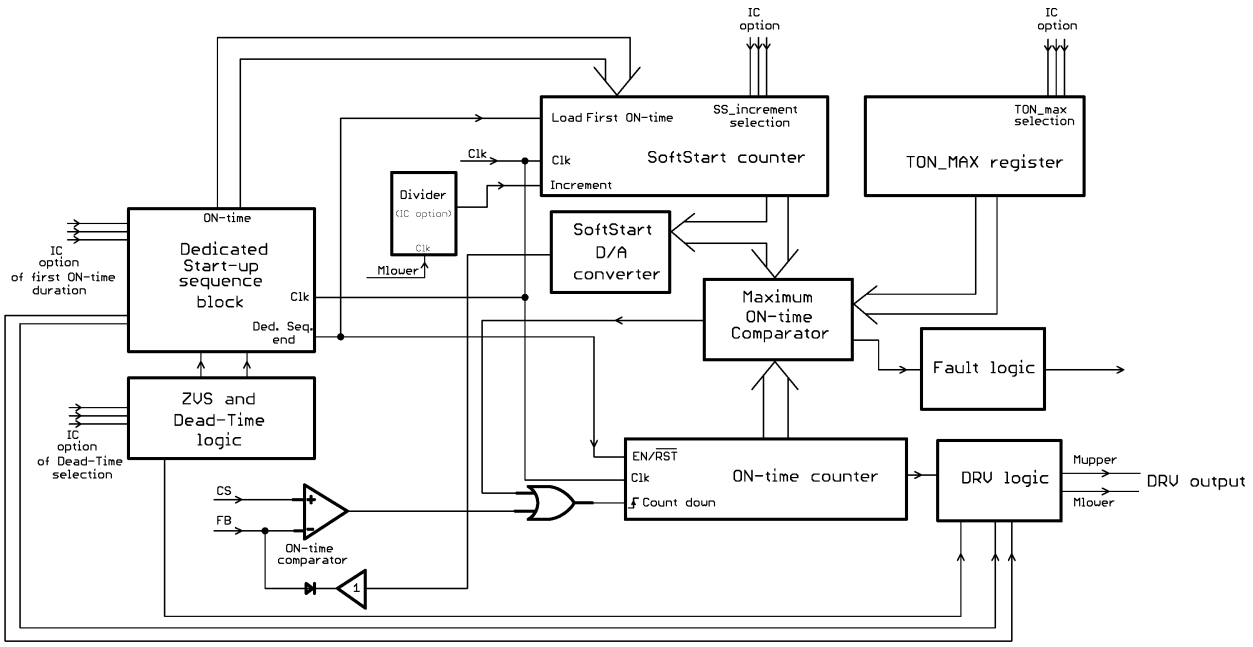


Figure 50. Soft−start Block Internal Implementation

The soft−start block subsystems and operation are described below:

1. The **Soft−Start counter** is a unidirectional counter that is loaded with the last Mupper on−time value that is reached at the dedicated startup sequence end (i.e. during condition b occurrence explained in previous chapter). The on−time period used in the initial period of the soft−start sequence is affected by the first Mupper on−time period selection and the dedicated startup sequence processing. The Soft−Start counter counts up from this initial on time period to its maximum value which corresponds to the IC maximum on−time. The Soft−Start counter is incremented by the soft−start increment number ($t_{SS_INCREMENT}$) during each Mlower switch on−time period. The soft−start start increment, selectable via IC option, thus affects the soft−start time duration. The Mlower clock signal for the Soft−Start counter can be divided down by the SS clock divider ($K_{SS_INCREMENT}$) in case the soft−start period needs to be prolonged further – this can be also done via IC option selection. The Soft−Start period is terminated (i.e. the counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB_SKIP_IN}$ level.
2. The **ON−time counter** is a bidirectional counter that is used as a main system counter for on−time modulation during soft−start, normal operation or overload conditions. The ON−time counter counts−up during Mupper switch conduction period and then counts down to zero – defining Mlower switch conduction period. This technique assures perfect 50 % duty cycle symmetry for both power switches as afore mentioned. The ON−time counter count−up mode can be switched to the count−down mode by either of two events: **1st** when the ON−time counter value reaches the maximum on−time value (t_{TON_MAX}) or **2nd** when the actual Mupper on−time is terminated based on the current sense input information.
3. The **Maximum ON−time comparator** compares the actual ON−time counter value with the maximum on−time value (t_{TON_MAX}) and immediately activates the latch (or auto−recovery) protection mode. The minimum operating frequency of the controller is defined the same way. The Maximum ON−time comparator reference is loaded by the Soft−Start counter value on each switching cycle during soft−start. The Maximum ON−time fault signal is ignored during Soft−Start operation. The converter Mupper switch on−time (and thus operating frequency) is thus defined by the Soft−Start counter value indirectly – via Maximum ON−time comparator. The Mupper switch on−time is increased until the Soft−Start counter reaches t_{TON_MAX} period and Maximum on−time protection is activated, or until ON−time comparator takes action and overrides the Maximum ON−time comparator.
4. The **Soft−Start D/A converter** generates a soft−start voltage ramp for ON−time comparator input synchronously with Soft−Start counter incrementing. The internal FB signal for ON−time comparator input is artificially pulled−down and then ramped−up gradually when soft−start period is placed by the system – refer to Figure 51. The FB loop is supposed to take over at certain point

when regulation loop is closed and output gets regulated so that soft−start has no other effect on the on−time modulation. The Soft−Start counter continues counting−up until it reaches its maximum value which corresponds to the IC maximum on−time value – i.e. the IC minimum operating frequency. The Soft−Start period is terminated (i.e. counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB_SKIP_IN}$ level. The D/A converter output evolve accordingly to the Soft−Start counter as it is loaded from its output data bus.

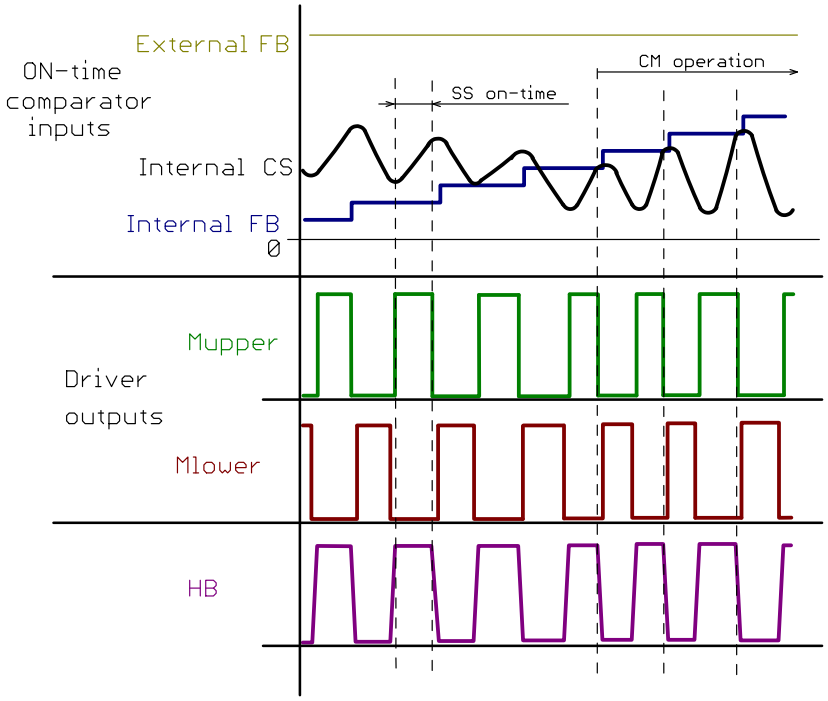


Figure 51. Soft Start Behavior

The Controller Operation during Soft−start Sequence Evolves as Follows:

The Soft−Start counter is loaded by last Mupper on−time value at the end of the dedicated startup sequence. The ON−time counter is released and starts count−up from zero until the value that is equal to the actual Soft−Start counter state. The Mupper switch is active during the time when ON−time counter counts−up. The Maximum ON−time comparator then changes counting mode of the ON−time comparator from count−up to count−down. A dead−time is placed and the Mlower switch is activated till the ON−time counter reaches zero value. The Soft−Start counter is incremented by selected increment during corresponding Mlower on−time period so that the following Mupper switch on−time is prolonged automatically – the frequency thus drops naturally. Because the operating frequency of the controller drops and Mlower DRV signal is used as a clock source for the Soft−start counter, the soft−start speed starts to decrease on each (or on each N−th) Mlower driver pulse (where N is defined by $K_{SS_INCREMENT}$) of switching cycle. So we have non−linear soft−start that helps to speed up output charging in the beginning of the soft−start operation and reduces the output voltage slope when the output is close to the regulation level. The output bus of the Soft−Start counter addresses the D/A converter that defines the ON−time comparator reference voltage. This reference voltage thus also increases non−linearly from initial zero level until the level at which the current mode regulation starts to work. The on−time of the Mupper and Mlower switch is then defined by the ON−time comparator action instead of the Maximum ON−time comparator. The soft−start then continues until the regulation loop is closed and the on−time is fully controlled by the secondary regulator. The Soft−Start counter then continues in counting and saturates at its maximum possible value which corresponds to IC minimum operating frequency. The maximum on−time fault detection system is enabled when Soft−Start counter value is equal to t_{TON_MAX} value.

The previous on−time repetition feature, described above in the ON−time modulation and feedback loop chapter, is disabled in the beginning of soft start period. This is because the ON−time comparator output stays high for several cycles of soft start period – until the current mode regulation takes over. The previous on−time repetition feature is enabled once the current modulation starts to work fully, i.e. in the time when the ON−time comparator output periodically drops to low state within actual Mupper switch on−time period. Typical startup waveform of the LLC application driven by NCP1399 controller can be seen in Figure 52.

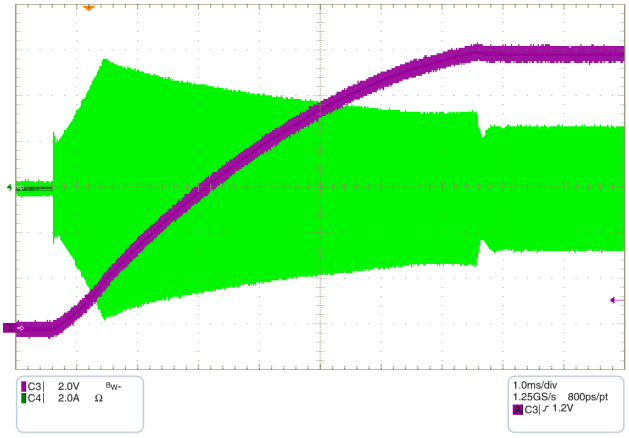


Figure 52. Application Startup with NCP1399 – Primary Current – green, V_{out} – magenta

Skip Mode Operation

An LLC resonant converter efficiency reaches high values under medium and full load conditions thanks to ZVS operation for the primary MOSFETs and ZCS operation for the secondary rectifiers. The light−load and no−load efficiency however drops unacceptably when a normal frequency modulation control technique is used. This is because the converter operating frequency needs to be increased quite a lot compared to nominal load operating frequency in order to maintain regulation under light load conditions. High operating frequency increases driving losses in the controller and also losses in the converter power stage. Moreover, the magnetizing current that becomes major primary current component during light load conditions, circulates in the resonant tank and creates power losses in the power switches despite minimum energy transfer to the secondary side. This is why the majority of resonant converter controllers implement skip mode operation under light load conditions.

The NCP1399 controller implements a proprietary skip mode technique that assures maximum light−load efficiency and low acoustic noise. The FB pin voltage level below which the application enters skip mode operation is fully user adjustable for the NCP1399A device family – via SKIP/REM adjust pin or via IC option for the NCP1399B device family. The skip mode operation can be initiated by the skip comparator only during actual Mupper driver on−time period. This technique assures defined and synchronous transition from normal to skip mode operation. The SKIP/REM pin voltage (NCP1399Ay) or internal voltage level (NCP1399By) defines the FB pin voltage threshold under which is the skip mode initiated – the maximum operating frequency of the converter is thus defined indirectly.

The Mlower switch is always activated for a defined on−time period at the beginning of each skip burst to re−charge the bootstrap capacitor and thus assure enough charge for high side driver powering during the following Mupper pulse. The resonant capacitor average voltage level is maintained below Vbulk/2 level during the skip mode operation. This technique helps to minimize power loses during the initial Mlower MOSFET switch activation – refer to Figure 53.

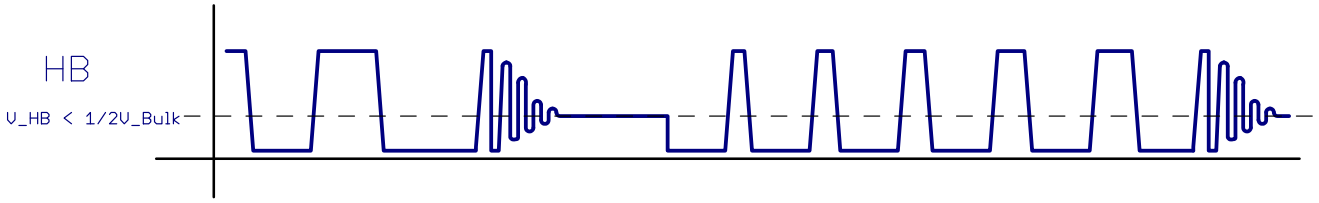


Figure 53. The average voltage of resonant capacitor is maintained below Vbulk/2 during the skip mode operation to reduce turn−on losses during 1st Mlower skip burst pulse

The first pulse in the skip burst is always non−ZVS because there is no magnetizing energy in the resonant tank that could prepare ZVS condition for lower MOSFET switch turn−on. The reduced resonant capacitor voltage thus helps to decrease C*V^2 losses related to the total HB line capacitance (composed from output capacitances of the power stage MOSFETs and stray capacitance seen by the HB line). However, too low of a resonant capacitor voltage, during 1st Mlower driver pulse initiation, would result in a too low resonant tank current at the end of the first Mlower switch conduction period and thus a non ZVS condition for the following Mupper switch turn−on process. This is why a full discharge of resonant capacitor is not needed before skip mode.

The reduced resonant capacitor average voltage requirement imposes a specific turn−off sequence to be used at the end of each skip burst and also during transition from normal operation mode to skip mode– refer to Figure 54. The Mlower driver is always activated the latest during transition to skip mode. However, the latest Mlower driver activation on−time is equal to 3/2 of previous Mupper pulse width when the skip mode is entered. This technique naturally imbalances the resonant tank so that the average resonant capacitor voltage stays below Vbulk/2 level. – i.e. application is prepared for optimal initialization of the following skip burst.

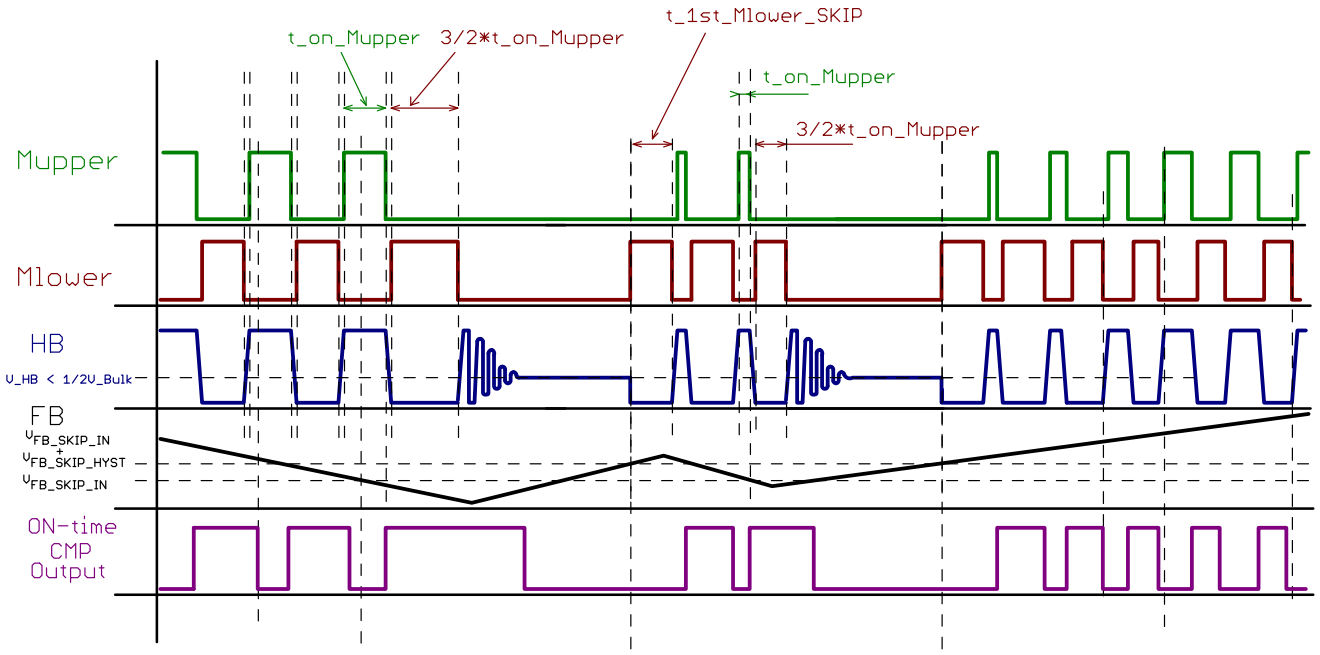


Figure 54. Drivers turn−off sequence during transition to skip−mode from normal operation mode

The voltage level across the resonant capacitor after the transition to skip mode depends on several factors:

- Actual previous Mupper switch on−time – i.e. actual operating frequency when skip mode comparator provides skip mode operation request to the internal logic via its output
- Resonant tank components used in the application
- Actual current flowing through the resonant tank when last Mlower driver pulse is initiated

It should be noted that the oscilloscope probe discharges the resonant capacitor by its resistance when connected to the HB pin! The probe discharge effect to the resonant capacitor is obvious when no−load is applied to the converter output and the application enters deep skip mode. This has to be taken into account when probing HB pin and operating application in skip mode.

The NCP1399 detects skip mode operation via FB voltage level. The skip comparator features an adjustable $V_{FB_SKIP_IN}$ threshold (externally with the NCP1399A device family or internally by IC option with the NCP1399B device family) and fixed hysteresis ($V_{FB_SKIP_HYST}$). The skip out level is thus given by $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ value – refer to Figure 55. The controller disables drivers and enters a low consumption mode once the FB voltage drops below $V_{FB_SKIP_IN}$ threshold. The IC operation is restarted once the $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ level is exceeded on the FB pin. As aforementioned, the controller then activates Mlower driver first for a predefined time ($t_{1st_MLOWER_SKIP}$) to re−charge the bootstrap capacitor. The first Mupper driver pulse is then placed by the controller after DT period elapsed. The on−time of the first Mupper pulse is dictated by the ON−time comparator – i.e. the on−time depends on the actual FB pin voltage and CS pin input signal. The internal FB signal is artificially reduced by $V_{1st_MUPPER_SKIP}$ via the ramp compensation block during this first Mupper driver pulse. This method helps reduce the primary current peak and acoustic noise during return from skip mode. The amount of internal FB signal and thus primary peak current compression is adjustable via IC option.

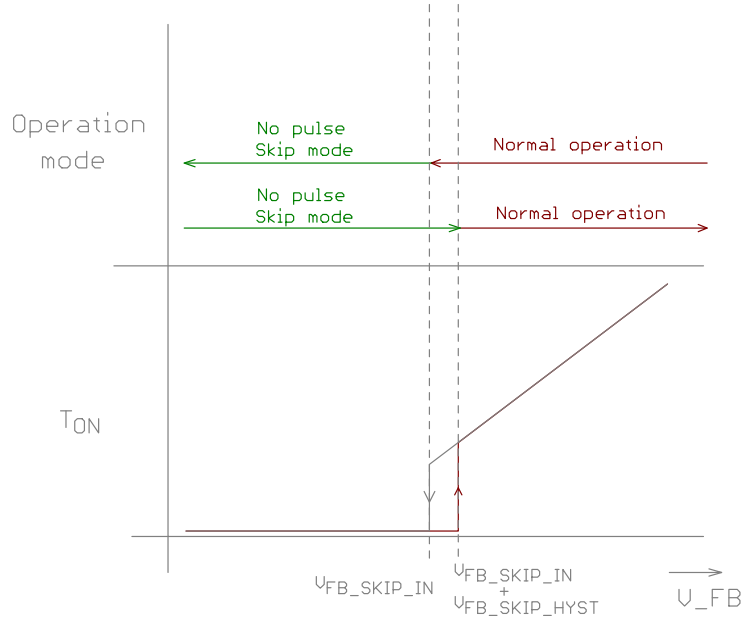


Figure 55. NCP1399 Light−load Operating Modes versus Feedback Pin Voltage

Detail Description of the Skip Mode Operation:

During operation under certain load conditions in normal PFM mode (driving the resonant tank with 50% DC symmetry), if the load drops, then the load current is reduced and the converter operation evolves as follows:

1. The FB voltage falls below the $V_{FB_SKIP_IN}$ threshold. This event can be detected by the system only during the Mupper switch on−time execution. The actual Mupper pulse on−time is stored into the dedicated t_Mu_on−time register. The last Mlower pulse with t_Ml_on−time = 3/2* t_Mu_on−time is introduced by the system to finish operation and will keep the resonant capacitor out of balance at a voltage below 1/2 of Vbulk. The controller then enters a low consumption mode in which all unnecessary blocks are turned off to reduce power consumption and the IC will waits as long as the feedback pin voltage stays above $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ level.
2. The FB pin voltage rises above $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ threshold. The first Mlower period with pre−defined on−time width ($t_{1st_MLOWER_SKIP}$) is placed in order to recharge the bootstrap capacitor. The first Mupper pulse is then initiated after a dead−time period that lasts until termination by the CS comparator. The dead−time period is then followed by second Mlower pulse which on−time period could differ based on the actual application conditions:
   b1) the second Mlower pulse with on−time equal to previous Mupper driver pulse period is placed in case that the ON−time comparator output is low before end of regular Mlower period.
   b2) the second Mlower pulse with on−time longer than previous Mupper driver pulse period is placed in case that the ON−time comparator output is high in the end of regular Mlower period. The second Mlower pulse is prolonged in such case until the ON−time comparator output gets low. This technique ensures that the current mode operation is not lost due to resonant capacitor voltage imbalance that naturally occurs during burst operation. The application works with asymmetrical duty cycle in this case.
3. The dead time is placed by the system again and situation from point b) repeats. The b2) case repeats in a given skip burst pulse until the duty cycle symmetry of 50% is reached i.e. until the b1) case is reached by the system. The asymmetrical operation is then disabled until the new $V_{FB_SKIP_IN}$ threshold crossing event, i.e. until the application enters skip mode again.
4. Application continues with given skip burst until the $V_{FB_SKIP_IN}$ threshold is reached on the FB pin. This situation is monitored during each Mupper driver period. The dead time is then placed by the driver followed by last Mlower driver pulse with on−time equal to 3/2 of previous Mupper driver period. The controller consumption is then minimized by turning−off all the blocks that are not needed. The skip comparator is monitoring FB pin voltage – waiting for new skip burst initialization.

Example of imbalanced operation during the skip mode burst beginning can be seen in Figure 56. One can see that the ON−time comparator output (Yelow) is high while Mlower on−time is equal to the previous Mupper pulse width – thus the Mlower on−time period is prolonged until the ON−time comparator output drops.

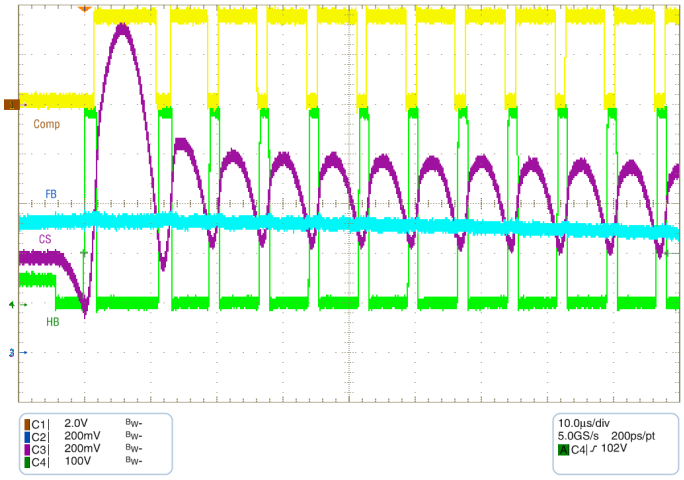


Figure 56. The on−time comparator prolongs Mlower periods in case it output is high after previous Mupper period is already exceeded on Mlower so imbalanced operation is placed by the system in order to keep current mode operation working. This functionality is active until the duty cycle symmetry reaches 50%.

Fast transition to skip mode can occur when the load current diminishes abruptly and the application is working in full load. The frequency then quickly increases which can result in resonant capacitor imbalance that could lead to a loss of current mode operation – refer to Figure 57 for illustration. This is why the NCP1399 repeats previous Mupper on−time period in case the ON−time comparator output does not drop low within this time period (i.e. within the time equal to last Mupper on−time).

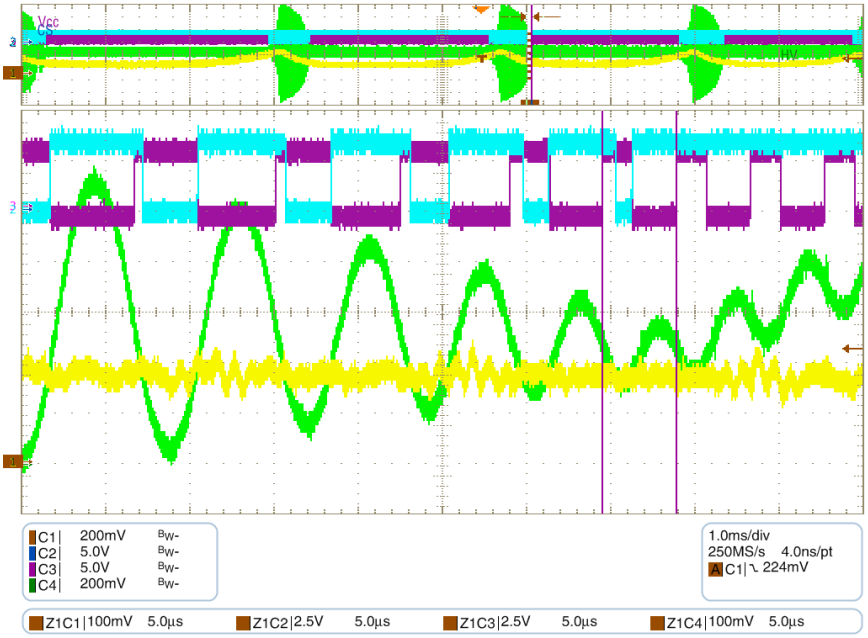


Figure 57. Mupper on−time repetition in case of transient loading when resonant capacitor imbalance occurs and on−time comparator output stays high for several periods.

Summary of the NCP1399 Skip Mode System Operation:

When the load slowly diminishes and the operating frequency of the LLC converter increases, skip mode with wide skip bursts is naturally placed by the system first – refer to Figure 58. The off−time between skip bursts increases and the number of pulses in skip burst drops when load is reducing further i.e. FB voltage starts to trigger the $V_{FB_SKIP_IN}$ + $V_{FB_SKIP_HYST}$ thresholds with lower frequency. The single pulse burst operation could be reached under no load on the output in systems with very fast feedback loop response. The skip burst composes only from single Mupper and two Mlower pulses in such case. The initial Mlower pulse width of skip burst is defined by device option and is used for bootstrap capacitor pre−charge and

ZVS condition preparation for following Mupper switch activation. The skip burst is always finished by the Mlower driver pulse with period prolonged to 3/2 of previous Mupper switch on time period in order to reduce resonant capacitor voltage and prepare system for another skip burst initialization.

The overall skip mode operation of the application is affected by several factors:

1. FB voltage skip in threshold adjust
2. FB voltage skip hysteresis
3. First Mlower DRV pulse width when IC is returning from skip mode
4. First Mupper pulse internal FB voltage reduction factor when IC is returning from skip mode
5. Actual bulk voltage value

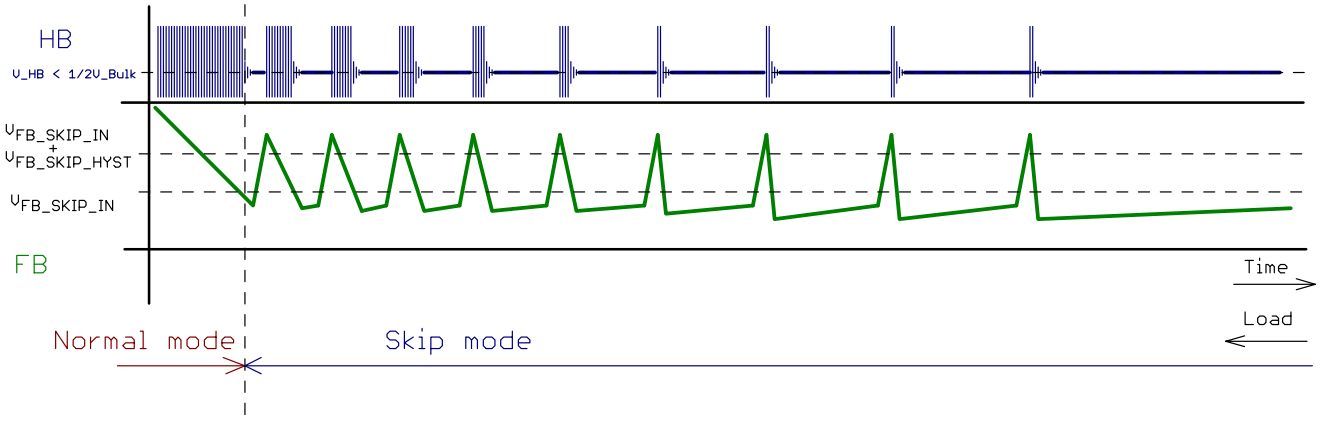


Figure 58. NCP1399 Operation when Load Current Drops Down to No−load Conditions

The High Voltage Half−bridge Driver

The driver features a traditional bootstrap circuitry, requiring an external high voltage diode with resistor in series for the capacitor refueling path. Minimum series resistor Rboot value is 3.3 Ω. Figure 59 shows the internal architecture of the drivers section. The device incorporates an upper UVLO circuitry that makes sure enough V_{GS} is available for the upper side MOSFET.

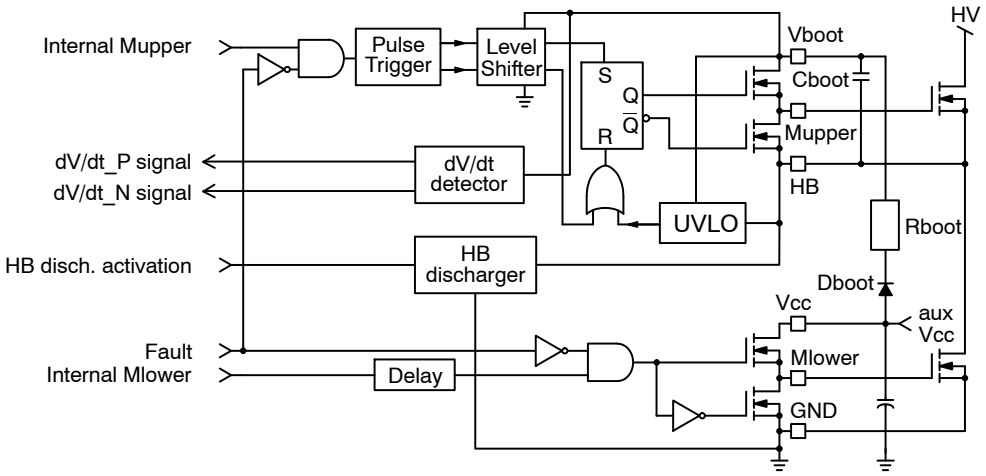


Figure 59. The NCP1399 Internal DRVs Structure

The internal dV/dt sensor, connected to the VBOOT pin, detects the HB pin voltage transitions in order to setup the optimum DT period – please refer to Dead−Time chapter. The internal HV discharge switch is connected to the HB pin and discharges resonant capacitor before application startup. The current through the switch is regulated to $I_{DISCHARGE}$ level until the V_{HB_MIN} threshold voltage is reached on the HB pin. The discharge system assures always the same startup conditions for application – regardless of previous operating state.

As stated in the maximum ratings section, the floating portion can go up to 620 VDC on the BOOT pin. This voltage range makes the IC perfectly suitable for offline applications featuring a 400 V PFC front stage.

Automatic Dead−time Adjust

The dead−time period between the Mupper and Mlower drivers is always needed in half bridge topologies to prevent any cross conduction through the power stage MOSFETs that would result in excessive current, high EMI noise

generation or total destruction of the application. Fixed dead−time period is often used in the resonant converters because this approach is simple to implement. However, this method does not ensure optimum operating conditions in resonant topologies because the magnetizing current is changing with line and load conditions. The optimum dead−time, under a given operating conditions, is equal to the time that is needed for bridge voltage to transition between upper and lower states and vice versa – refer to Figure 60.

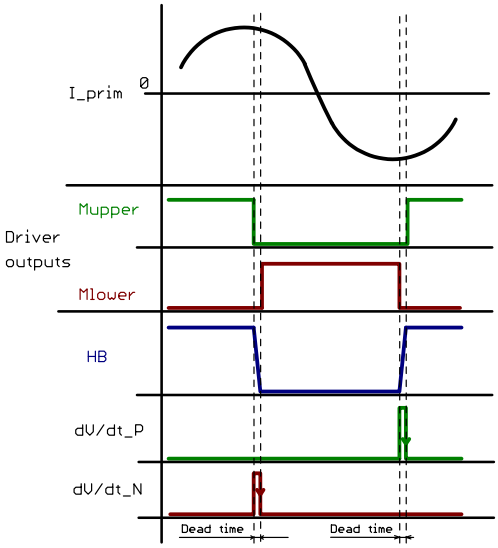


Figure 60. Optimum Dead−time Period Adjust

The MOSFET body diode conduction time is minimized when optimum dead−time period is used which results in maximum efficiency of a resonant converter power stage. There are several methods to determine the optimum dead−time period or to approximate it (for example using auxiliary winding on main transformer or modulating dead−time period with operating frequency of the converter). These approaches however require a dedicated pin for nominal dead−time adjust or auxiliary winding voltage sensing. The NCP1399 uses a dedicated method that senses the VBOOT pin voltage internally and adjusts the optimum dead−time period with respect to the actual operating conditions of the converter. The high−voltage dV/dt detector, connected to the VBOOT pin, delivers two internal digital signals that are indicating Mupper to Mlower and Mlower to Mupper transitions that occur on the HB and VBOOT pins after the corresponding MOSFET switch is turned−off. The controller enables the opposite MOSFET in the power stage once the corresponding dV/dt sensor output provides information about HB (or VBOOT) pin transition ends.

The ZVS transition on the bridge pin (HB) could take a longer time or even does not finish in some cases – for example with extremely low bulk voltage or when some critical failure occurs. This situation should not occur normally in correctly designed application because several other protections would prevent such a situation. The NCP1399 implements maximum DT period clamp that limits driver's off−time period to the $t_{DEAD_TIME_MAX}$ value. The corresponding MOSFET driver is forced to turn−on by the internal logic regardless of missing dV/dt sensor signal. This situation does not occur during normal operation and will be considered a fault state by the device. There are several possibilities on how the controller continues operation after this event occurrence – depending on the IC option:

1. The opposite MOSFET switch is forced to turn−on when $t_{DEAD_TIME_MAX}$ period elapses and no fault is generated
2. The controller is latched−off in case the ZSV condition is not detected within selected $t_{DEAD_TIME_MAX}$ period
3. The controller stops operation and restarts operation after auto−recovery period in case the ZSV condition has not been detected within the selected $t_{DEAD_TIME_MAX}$ period

A DT fault counter option is available. Selected number (N_{DT_MAX}) or DT fault events have to occur in order to confirm DT fault in this case.

A fixed DT option is also available for this device. The internal dV/dt sensor signal is not used for this device option and the $t_{DEAD_TIME_MAX}$ period is used as a regular DT period instead. The DT fault detection is disabled in this case.

Temperature Shutdown

The NCP1399 includes a temperature shutdown protection at 150°C. The typical TSD hysteresis is 30°C. When the temperature rises above the upper threshold, the controller stops switching instantaneously, and goes into the off−mode with extremely low power consumption. The V_{CC} supply is maintained (by operating the HV start−up in DSS mode) in order to memorize the TSD event information. When the temperature falls below the lower threshold, the full restart (including soft−start) is initiated by the controller. The HV startup current source features an independent over−temperature protection which limits its output current in case the DIE temperature exceeds 150°C to avoid damage to the HV startup silicon structure.

APPLICATION INFORMATION

Controller Operation Sequencing of NCP1399xy LLC Controller

The paragraphs below describe controller operation sequencing under several typical cases as well as transitions between them. The NCP1399By version is used in the description of most operation sequences (except last paragraph, Figure 65 that describe NCP1399Ay version). The main behavior of NCP1399Ay is as same as NCP1399By version except for the off−mode behavior (REM pin function).

1. Application start, Brown−out off and restart, OVP/OTP latch and then restart – Figure 61

Application is connected to the mains at point **A** thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until V_{CC} reaches V_{CC_ON} threshold.

The VCC pin voltage reached V_{CC_ON} threshold in point **B**. The BO, FB, OVP/OTP and PFC MODE blocks are enabled. The REM input is internally pulled down for t_{REM_TIMER} to assure that the secondary side will have enough time to recover normal operation and pulls down the remote optocoupler after the LLC stage restart. The VBULK/PFC FB pin starts to receive divided bulk voltage as the external HV switch is activated by PFC MODE output. The REM timer is activated during each V_{CC_ON} event except during the off−mode operation. The V_{CC} blank is also activated during each V_{CC_ON} event to ensure that the internal logic ignores all fault inputs until the internal blocks are fully biased and stabilized after a V_{CC_ON} event. The IC DRVs were not enabled after first V_{CC} blank period in this case as the voltage on VBULK/PFC FB is below V_{BO} level. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the fault conditions is still present.

The BO_OK condition is received (voltage on VBULK/PFC FB reach V_{BO} level) at point **C**. The IC activates the startup current source to refill VCC capacitor in order to assure sufficient energy for a new startup. The VCC capacitor voltage reaches V_{CC_ON} level again and the VCC blank period is started. The REM timer is activated again on this V_{CC_ON} event as well. The DRVs are enabled and the application is started after V_{CC} blank period lapses because there is no faults condition at that time.

Line and also bulk voltage drops at point **D** so the BO_OK signal become low (voltage on VBULK/PFC FB drops below V_{BO} level). The LLC DRVs are disabled as well as OVP/OTP block bias. The PFC MODE output stay high to keep the bulk voltage divider connected, so the BO block still monitors the bulk voltage. The controller activates the HV startup current source into DSS mode to keep enough VCC voltage for operation of all blocks that are active while the IC is waiting for BO_OK condition.

The line voltage and thus also bulk voltage increase at point E so the Brown−out block provide the BO_OK signal once the V_{BO} level is reached. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart.

The V_{CC_ON} level is reached in point **F**. The OVP/OTP block is biased, REM timer and the VCC blank period is started at the same time. The controller restores operation via the regular startup sequence and soft−start after VCC blank period lapses since there is no fault condition detected.

The application then operates normally until the OVP/OTP input is pulled−up at point **G**. The controller then enters latch−off mode in which all blocks are disabled except for the feedback block. The VCC management controls the HV startup in DSS mode in order to keep enough VCC level to hold the latch−up state memorized while the application remains plugged−in to the mains.

The power supply is removed from the mains at point **H** and the VCC voltage drops down below V_{CC_RESET} level thus the low voltage controller is released from latch. A new application start occurs when the user plugs the application the mains again.

2. Application start, Brown−out off and restart, output short fault with auto−recovery restart – Figure 62

Operating waveforms descriptions for this figure is similar to one for Figure 61 from point **A** till point **G** – with one difference. The skip mode operation (FB < $V_{FB_SKIP_IN}$) blocks the IC startup after first V_{CC_ON} event instead of BO_fault.

The LLC converter operation is stopped in point **G** because the controller detects an overload condition (short circuit event in this case as the Vout drops abruptly). The controller disables all blocks except for the FB block and the fault logic. The HV startup DSS operation is initiated in order to keep enough VCC level for all internal blocks that need to be biased. Internal auto−recovery timer counts down the recovery delay period t_{A-REC_TIMER}.

The auto−recovery restart delay period lapses at point **H**. The HV startup current source is activated to recharge VCC capacitor before a new restart.

The V_{CC_ON} threshold is reached in point **I** and all the internal blocks are biased. The V_{CC} blank, REM timer and OVP/OTP blank period are started at the same time. The LLC converter operation is enabled, including a dedicated startup and soft−start period. The output short circuit is removed in between thus the Vout ramped−up and the FB loop took over during the LLC converter soft−start period.

3. Startup, skip−mode operation, low line detection and restart into skip−mode – Figure 63

The application is plugged into the mains at point **A** thus the HV input of the controller becomes biased. The HV startup current source starts charging the VCC capacitor until V_{CC} reaches the V_{CC_ON} threshold.

The VCC pin voltage reaches the V_{CC_ON} threshold at point **B**. The BO, FB, OVP/OTP and PFC MODE blocks are enabled. The REM input is pulled down for t_{REM_TIMER} to assure that the secondary side will have enough time to recover to normal operation and pulls down the remote optocoupler after the LLC stage restarts. The VBULK/PFC FB pin begins to receive divided bulk voltage as the external HV switch is activated by the PFC MODE output. The V_{CC} blank period is activated during each V_{CC_ON} events. This blank ensures that the internal logic ignores all fault inputs until the internal blocks are fully biased and stabilized after V_{CC_ON} event. The IC DRVs are not enabled even after V_{CC} blank period ends because the OVP fault condition is present. The OVP fault condition disappears after some time so the HV startup current source is enabled to prepare enough V_{CC} for a new startup attempt. The new V_{CC} blank, OTP blank and REM timer periods are placed after the

V_{CC_ON} event is detected. The controller authorizes DRVs at point **C** as there are no faults conditions present after the V_{CC} blank period lapses.

The application is operating under certain load conditions between points **C** and **D**. The load current is reduced thus the FB loop reduces the primary controller FB pin voltage. The PFC controller is disabled (via reduced voltage on the PFC MODE pin to $V_{PFC_M_BO}$ value) in point **D** when the FB pin voltage drops below set voltage level on P ON/OFF pin.

The load diminished further and the FB skip threshold is reached in point **E**. The controller turns−off all the blocks that are not essential for the controller operation during skip−mode – i.e. all blocks except FB block and VCC management. This technique is used to minimize the device consumption when there are no driver pulses during skip−mode operation. The output voltage then drops naturally and the FB loop reflects this change into the primary FB pin voltage that increases accordingly. The auxiliary winding is refilling VCC capacitor during each skip burst thus the controller is supplied from the application during the skip mode operation.

The controller FB skip−out threshold is reached in point **F;** the controller enables all blocks and LLC DRVs to refill the output capacitor. The controller did not activate the HV startup current source because there is enough voltage present on the VCC pin during skip mode. The OTP blank periods is activated at the beginning of the skip burst to mask possible OTP faults.

Note: The VCC capacitor needs to be chosen with a value high enough to ensure that V_{CC} will not drop below the V_{CC_OFF} level during skip mode. The device would otherwise restart operation via standard startup sequence in such a case (i.e. ramp−up the V_{CC} to V_{CC_ON} level first and enable drivers afterwards) for NCP1399By version or enters into off−mode for NCP1399Ay (refer to Figure 65).

The line voltage drops in point **G,** but the bulk voltage is dropping slowly as there is nearly no consumption from the bulk capacitor during skip mode – only some refilling bursts are provided by the controller. The application thus continues in skip mode operation for several skip burst cycles.

The bulk voltage level less than V_{BO} threshold is detected by the controller in point **H** during one of the skip burst pulses. The controller thus disabled DRVs and enters DSS mode of operation in which the OVP/OTP block is disabled and the controller is waiting for BO_OK event. The PFC MODE provides the $V_{PFC_M_ON}$ voltage in this case to allow the PFC stage to refill bulk capacitors.

The line voltage is increased at point **I** thus the controller receives the BO_OK signal. The BO_OK signal is received during the period in which the HV startup current source is active and refills the VCC capacitor.

This V_{CC_ON} threshold is reached by the VCC pin at point **J**. The V_{CC} blank period, OVP/OTP blank and REM timer period are started at the same time. The full startup sequence is enabled at the end of the V_{CC} blank period as no fault is detected. The application then enters skip mode again as the load current is low.

5. Start−up, normal operation, transition to off−mode operation and output re−charge in off−mode (NCP1399By versions) – Figure 64

Application is connected to the mains at point **A** thus the HV input of the controller become biased. The HV startup current source starts charging the VCC capacitor until V_{CC} reaches V_{CC_ON} threshold.

The VCC pin voltage reached V_{CC_ON} threshold at point **B**. The BO, FB, OVP/OTP and PFC MODE blocks are enabled. The REM input is pulled down for t_{REM_TIMER} to ensure that the secondary side has enough time to recover normal operation and pull down the remote optocoupler after LLC stage restarts. The VBULK/PFC FB pin starts to receive the divided bulk voltage as the external HV switch is activated by the PFC MODE output. The V_{CC} blank period is activated during each V_{CC_ON} event. This blank ensures that the internal logic ignores all fault inputs until the internal blocks is fully biased and stabilized after V_{CC_ON} event.

The IC DRVs are enabled immediately after V_{CC} blank period ends as there was no fault present at that time. The application is operating under certain load conditions between points **C** and **D**. The load current is reduced thus the FB loop lowers the primary controller FB pin level. The PFC controller is disabled (via reduced voltage on the PFC MODE pin to $V_{PFC_M_BO}$ value) at point **D** when the FB pin voltage drops below the set voltage level on the P ON/OFF pin.

The secondary controller activates off−mode operation thus the REM input voltage exceeds the V_{REM_OFF} threshold at point **E**. The controller turns−off all the blocks that are not essential for controller operation during off−mode – i.e. all blocks including FB block and a large portion of the VCC management. This technique is used to minimize device consumption when there are no driver pulses during off−mode operation. The output voltage is then dropped naturally due to secondary controller and resistive dividers consumption. The primary controller is supplied from the HV startup current source that is operated in DSS.

The secondary controller interrupts off−mode operation by activating a remote optocoupler and pulling down the REM pin at point **F**. The controller activates HV startup current source and recharges the VCC capacitor to prepare enough V_{CC} voltage for new startup.

The V_{CC} voltage reaches V_{CC_ON} threshold at point **G** and the LLC converter starts (including soft−start) immediately after a V_{CC} blank period ends as there is no fault detected at the end of this period.

The output voltage is ramped up while the FB loop is not closed yet as the V_{OUT} is still below regulation level. The output voltage then reaches regulation level and the FB pin voltage drops abruptly on the primary – hitting the FB

skip−in threshold at point **H**. The LLC drivers are thus disabled by skip comparator. The FB then increased naturally – calling for new skip burst (refer to skip mode operation description in previous part).

Secondary controller activates the off−mode operation by releasing the remote optocoupler while the primary controller is operating in skip−mode. The REM pin voltage thus increases slowly up and hit the V_{REM_OFF} threshold where the primary controller enters off−mode operation again at point **I**.

6. Start−up, normal operation, transition to off−mode operation and output re−charge in off−mode (NCP1399Ay versions) – Figure 65

Operating waveforms descriptions for this figure are the same as for Figure 64 from point **A** until point **D** – Please refer to Figure 64 for details regarding operation between these time events.

The secondary controller activates off−mode operation by pulling FB pin below $V_{FB_REM_OFF}$ level, thus the IC goes into skip−mode for long time at point **E**. The controller turns−off all the blocks that are not essential for controller operation during skip−mode – i.e. all blocks except FB, BO and VCC management blocks. This technique is used to minimize device consumption when there are no driver pulses during skip−mode operation.

The V_{CC} drops naturally by IC consumption below V_{CC_OFF} threshold at point **F** – i.e. the off−mode is confirmed. The controller turns−off all the blocks that are not essential for controller operation during off−mode – i.e. all blocks including FB block and big portion of the VCC management. This technique is used to minimize device consumption when there are no drive pulses during off−mode operation. The output voltage is then dropped naturally due to secondary controller and resistive dividers consumption. The primary controller is supplied from the HV startup current source that operates in DSS mode.

The secondary controller interrupts off−mode operation by releasing the optocoupler and allowing the voltage on FB pin to ramp−up by the internal pull−up current source at point **G**. The controller activates the HV startup current source and recharges the VCC capacitor to prepare enough V_{CC} voltage for a new startup.

The V_{CC} voltage reaches V_{CC_ON} threshold at point **H** and the LLC converter starts (including soft−start) immediately after a V_{CC} blank period ends as there is no fault detected at the end of the period.

The output voltage is ramped up while the FB loop is not closed yet as the V_{OUT} is still below regulation level. The output voltage then reaches regulation level and the FB pin voltage drops abruptly on the primary – hitting the FB skip−in threshold at point **I**. The LLC drivers are thus disabled by the skip comparator. The FB then increases naturally – calling for new skip burst (refer to skip mode operation description in previous text).

The secondary controller activates off−mode operation by pulling−down FB pin and V_{CC} voltage naturally drops below V_{CC_OFF} threshold. The primary controller enters off−mode operation again at point **J**.

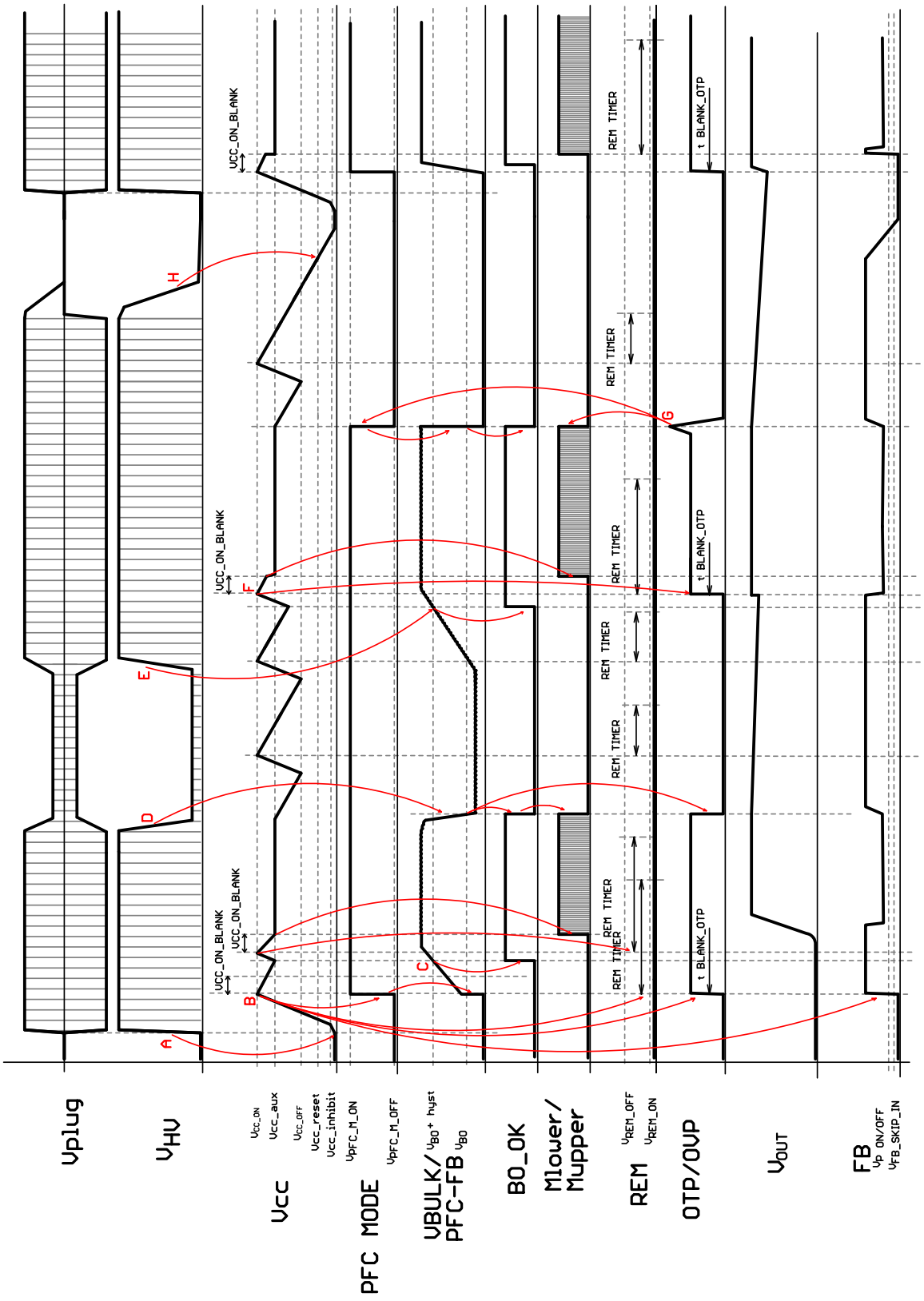


Figure 61. Application Start, Brown−out Off and Restart, OVP/OTP Latch and then Restart

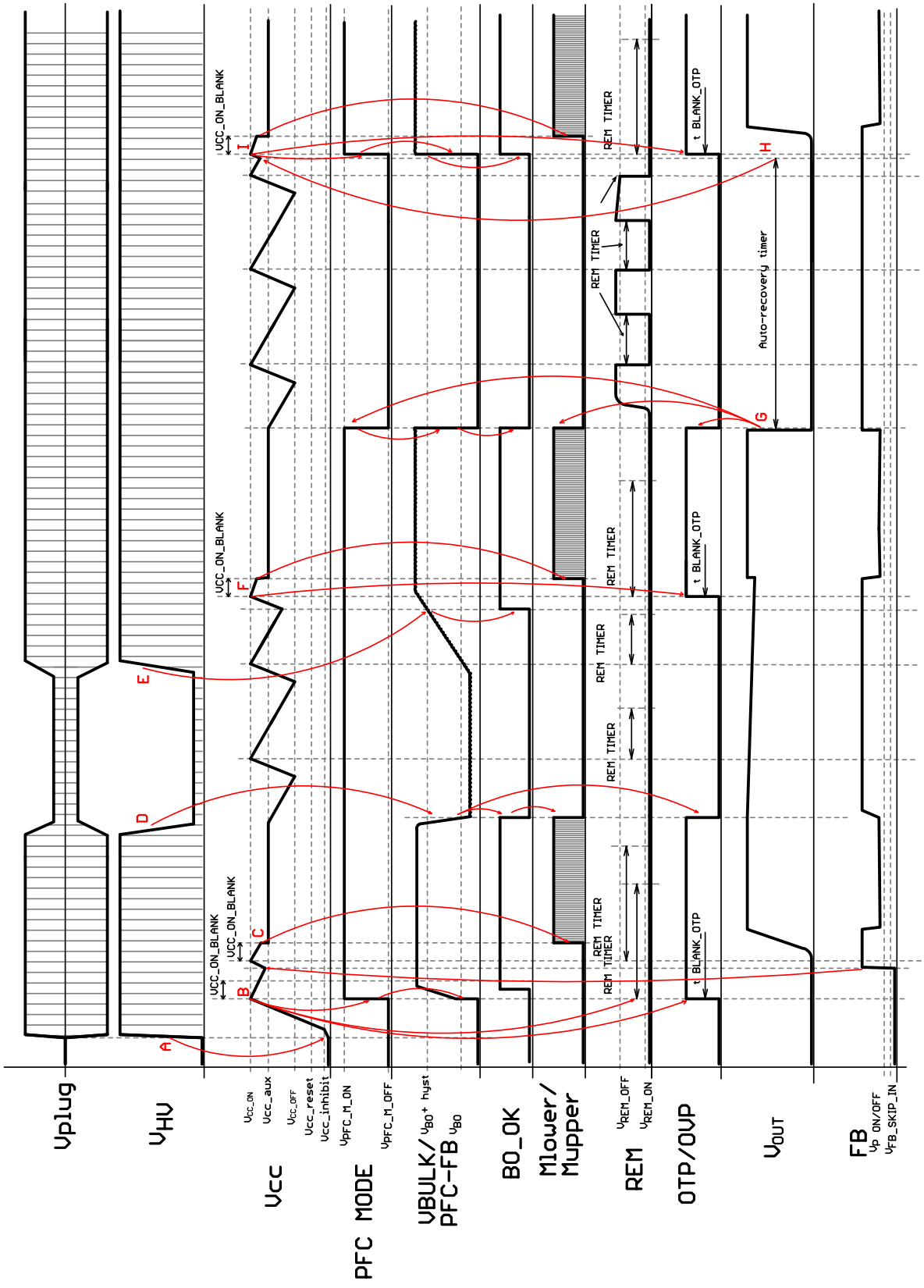


Figure 62. Application Start, Brown−out Off and Restart, Output Short Fault with Auto−recovery Restart

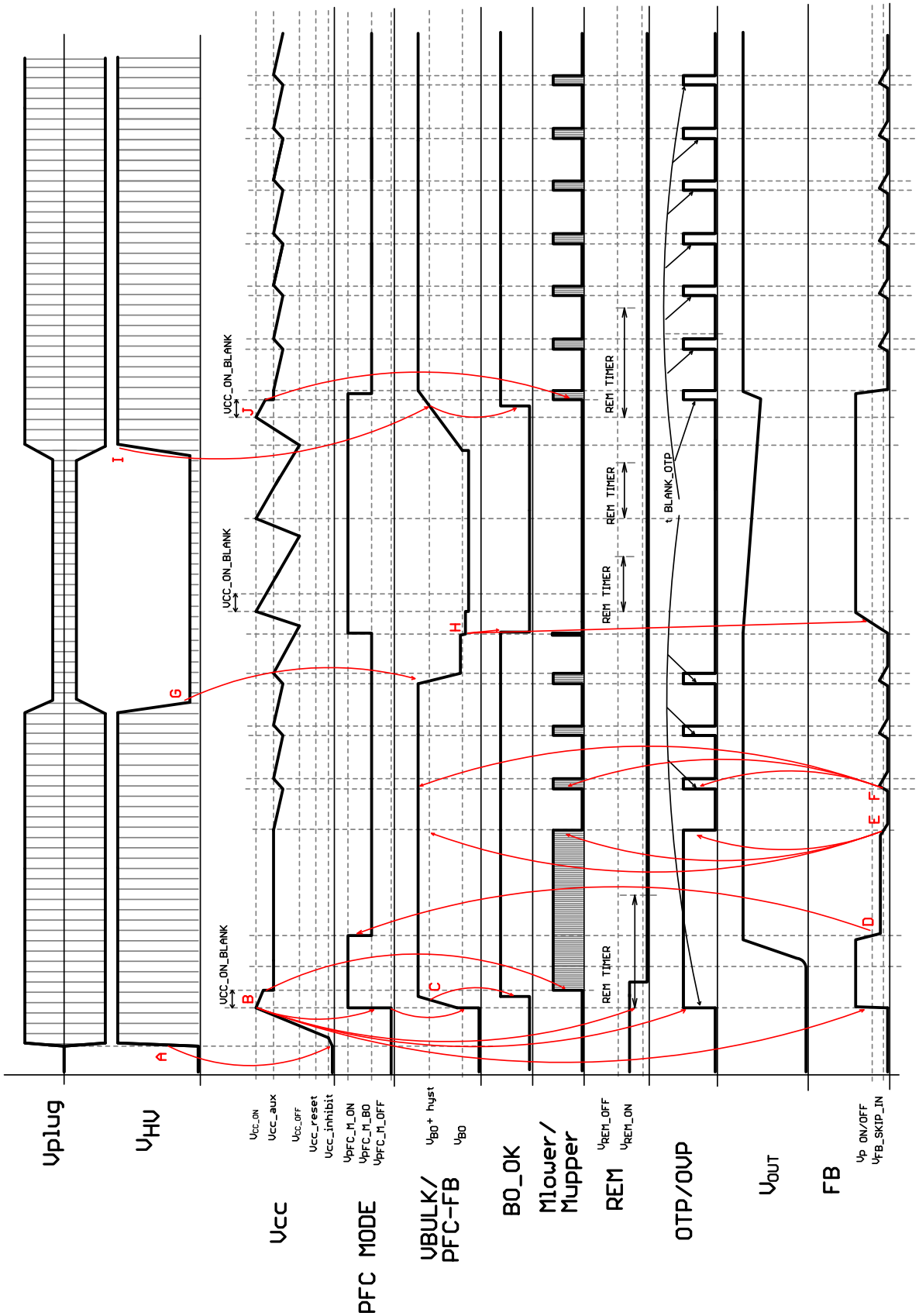


Figure 63. Startup, Skip−mode Operation, Low Lone Detection and Restart into Skip

Figure 64. Start−up, Normal Operation, Transition to Off−mode Operation and Output Re−charge in Off−mode – NCP1399By Version

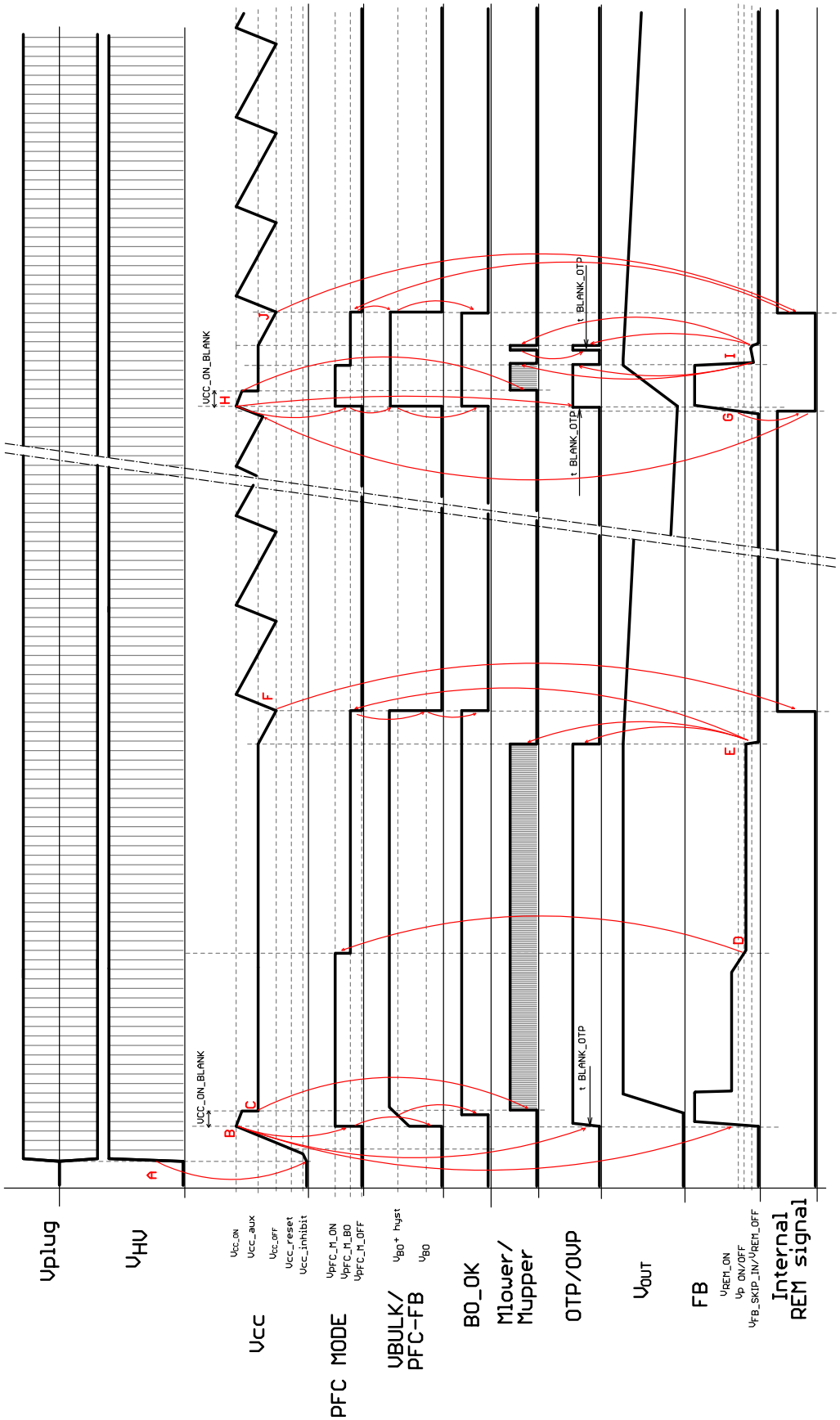
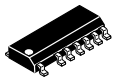


Figure 65. Start−up, Normal Operation, Transition to Off−mode Operation and Output Re−charge in Off−mode – NCP1399Ay Version



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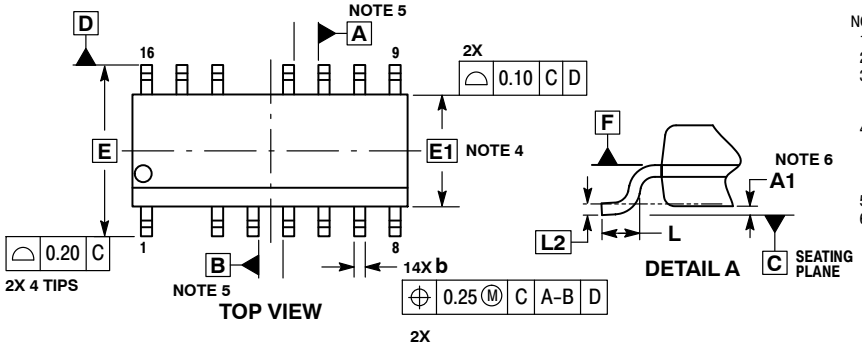
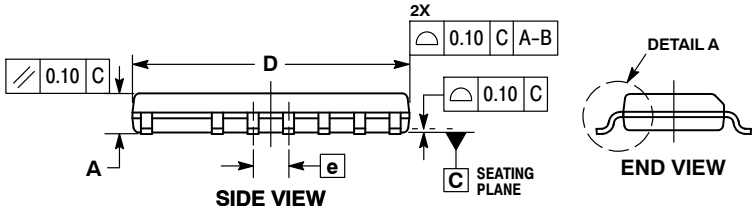
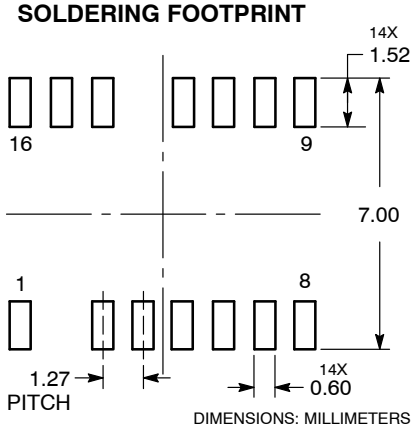




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

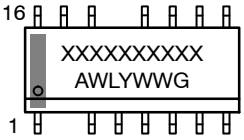
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
c	0.17	0.25
D	9.80	10.00
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.203 BSC	

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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